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Machine Learning-Augmented PPA Prediction Models for Early Floorplanning Decisions

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Abstract : Integrated circuit (IC) embedded design and constraints suggested by the advanced technology node have been found to accelerate the relevance of accuracy during the estimation of the power, performance, and area (PPA) metrics in the early phases of the design process in the floorplanning process. The ease of the then-existing Electronic Design Automation (EDA) tools could not be foreseeable as well as adaptable enough to simplify the PPA in the initial stages of designs and had to contain lengthy cycling and sub-optimum solutions. The recent developments in the sphere of machine learning (ML) have suggested radical equations on the basis of which one can learn by using already prepared design data and make real early predictions. The context of the present review is the discussion of the current research works that were performed in the field of machine learning-related models of PPA prediction, particularly when the environment is the first stage of the floorplanning decision-making. They consist of reinforcement-based learning used on adaptive placement, graph neural networks used on cross-stage PPA modeling, RTL-level delay prediction, and end-to-end optimization schemes. The entire progression of events is an enormous massive paradigm shift in chip design, smart and predictive, and the implication such will have on the effectiveness of the design industry and scalability and optimality of performance in the next generation EDA tools is merely gigantic.

IndexTerms **- Machine Learning, Floorplanning, PPA Prediction, VLSI Design**

1. Introduction

Not only has integrated circuit design been complex, but also a reduction in technology nodes has led to the need to devise design techniques that would allow the design to be in a position to accommodate the power, performance, and area (PPA) trade-offs at the design's beginning stage. The floorplanning is one of the things to be considered because it defines the physical structure of a chip on the whole. The congestion would lead to power distribution, signal integrity, and timing closure issues due to decisions made at this stage. These stakes render it high-value during the current times to be able to make the right predictions of PPA metrics. Nevertheless, the conventional Electronic Design Automation (EDA) systems, which are highly heuristic in nature, are not able to explore large dimensional design spaces in an efficient manner and may consume vast amounts of computing resources to obtain an output.

Machine learning (ML) and its capability to detect associations that are not easy to notice and, more importantly, being trained on previous data, is becoming a potential solution that can be used to complement the traditional EDA tools. In particular, ML can predict PPA measures at the preliminary design stages and preempt the results so as to achieve improved convergence and reduced design stages. Design tools are self-optimizing, adaptive, and predictive and provide an alternative paradigm that is introduced by the union of ML and EDA. The survey focuses on the most recent research works that implement machine learning to help with the PPA estimation and optimization in cases whereby the early floorplanning is applied. All the eight sources mentioned have been taken into account and summarized to provide deep knowledge of the existing practices, how they are used, and the new trend.

2. Theoretical Foundations and Transition to ML-based EDA

The classical EDA tools are designed to be constructed in a linear and iterative manner which eliminates the register-transfer level (RTL) specifications to layout, in a series of abstraction layers. Logic synthesis: The logic synthesis is not done in parallel, and all feedback control of the logic is usually by human beings. Placement: It is placed in sequence, and all the stages are often under human control. Clock tree synthesis: The clock tree is synthesized in a sequence, and the feedback control of the clock tree is usually under human control. Routing and signoff validation: Routing and signoff validation are done in a chronological sequence, and all the processes are normally regulated by humans. Such an anarchic form of working order reflects a negative influence on inefficiencies in the field of optimization of PPA measures in particular. This paradigm started to shift when machine learning appeared, and design flow provides a data-driven and predictive process today.

The first suggestion of such change is the one that presupposes that there is an application of ML to the field of logic synthesis. Machine learning has also affected the decision-making of synthesis that directly affects PPA, like mapping technology and gate sizing. Development of systems that can learn by design pattern patterns and make intelligent decisions have been proposed by reinforcement learning and data augmentation in regards to ways to optimize circuits. It has provided the neural network and the graph-based model with an indirect indication that it can optimize the PPA not only by supplying decision-making in the process of individual reasoning but also by how the process of reasoning can interface with the other processes that constitute the overall floorplan [1].

3. ML Applications in Floorplanning and Physical Design

The floorplan stage is an intricate stage on its own since it entails attaching the space designation of the different design elements besides taking into account the performance limitations and manufacturability limitations. The use of this type of machine learning is very useful because maybe it can provide forecasting facts of the future implications like bottlenecks or power wastage in the design that may be conveyed in the design decisions.

ML has been used in the floorplanning medium of the supervised, unsupervised, and reinforcement learning. Supervised learning in the physical design has been useful in predicting the wirelength, congestion, and timing metrics prediction of the obtained features on the early placement data and the RTL data. Furthermore, reinforcement learning has assisted tools in discovering or planning for floorplanning in an environment that involves continuous changes of the plans. The superiority of these adaptive systems is due to the fact that they are faster than the traditional optimization algorithms since they are trained policies, which can be applied in a wide variety of netlists and design settings [2].

Another aspect of the input to this direction is the model of floorplanning, and the PPA items are regarded as parallel objectives. The strategy enables the prediction model to get the trade-offs between the area minimization and timing closure as opposed to the optimal trade-offs. In the modern application of ML piping, as shown in Figure 1, forecasting and optimization processes have been incorporated in the cycle as a way of cutting the costly design cycles. It is a feedback system that is aided by graph neural networks and attention systems to discover suboptimal layouts within a restricted time and undertake remedial measures until they permeate through the design pipeline [2].

4. Reinforcement Learning for Early-Stage Optimization

Reinforcement learning (RL) is most effectively used in optimal control problems, which ought to have a design agent incorporated into the environment (in the present case, the chip layout) and subjected to the implementation of optimum decisions based on feedback. The use of RL, which contains block-placing and interconnecting—which have dire consequences on the outcome of PPA—has gone as far as to make decisions on the first level.

The fact that the capability to generate placement solutions with a low total wirelength and area and, at the same time, can generate decent performance has proven that RL-based agents are more efficient than other more traditional methods of heuristics. Rather than being forced to correct placing policies, the transfer of placing policies across designs can be learned by encoding the design state as a graph-structured representation and encoding the reward functions as functions of PPA measures respectively, by the learning of RL agents. To a great extent, the models can decrease the level of human involvement and make the tools of the trial as simple as possible [3].

The effective RL mechanism will be provided with information gained during the previous experience of floorplanning, thus enabling architecture design generalization. As an illustration, the trained RL agent is in a position to learn the effect of a macro placement nearby a net with a high fanout without timing or routing simulation. It is a hierarchical forecast in a hierarchical design flow and minimizes close time cycles in the process; thus, the layout inefficiency can be corrected at the initial level [3].

5. Predictive Modeling of Cross-Stage Design Metrics

The other, more modern form of ML-augmented EDA is the incorporation of cross-stage prediction models forming the linkage between the initial design decisions and the post-layout results. Previously, any change done in one of the designing processes like synthesis or floorplanning would be indeterministically communicated to the other stages of designing, like placement and routing. Machine learning can provide a chance to predict such consequences and control the former ones.

It has suggested a hybrid architecture in which every stage of the physical design (synthesis, floorplanning, placement, and routing) is represented by a graph neural network and boosted decision tree system. The models are founded on the RTL-level attributes and provide an approximation of the measures of such attributes as total negative slack (TNS), worst negative slack (WNS), power, and area. This is a multi-level combination of machine learning, and it enables the optimization of the flow to be harmonized. Figure 2 shows a design of such a system with reinforcement learning and prediction modules and parameter tuning to create a closed loop to give optimization of design results [4].

The consequences of such structures, as pertains to cross-stage predictability, have been of the nature that convergence time and the whole PPA have all been highly enhanced. Skilled cross-stage ML models in systems, which had the potential to accomplish this, allowed a reduction in the design cycle by at least 30 percent and area reduction by more than 20 percent [4].

6. Enhanced Placement through ML-Augmented Techniques

Flooring placement optimization, or floorplanning, is a method of floorplanning with effects on interconnect delay, congestion, and heat patterns. Among the biggest challenges, one should note the possibility to foresee the effects of the made decisions at a very young age on the effectiveness of the subsequent stages of the flow. ML-based techniques attempt to resolve this on the basis of feature maps, netlists, cell placement, and routing congestion.

The machine learning models are also trained to give their suggestions on the quality of position, and the prediction-based logic can be extended on the predictions. The models are anchored on the following properties: the density of reasoning, net criticality, and pin distribution, which renders the computation of the impact of the placement strategies on timing and power usage feasible. In comparison, the measured and estimated sources of power consumption curve of the converse design in Figure 3 below show that ML is an effective way of determining performance, in that it does not need to be applied in the real world [5].

Figure 1 illustrates the sequential flow of an ML-augmented design process from RTL input to PPA feedback through prediction and reinforcement learning.

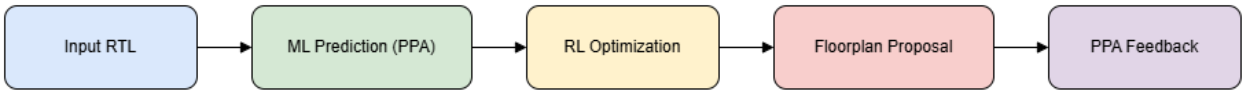

Figure 1: Workflow of an ML-augmented design flow showing integration of prediction, RL, and optimization [2]

Figure 2 presents a modular cross-stage pipeline where machine learning components collaboratively optimize floorplanning and placement.

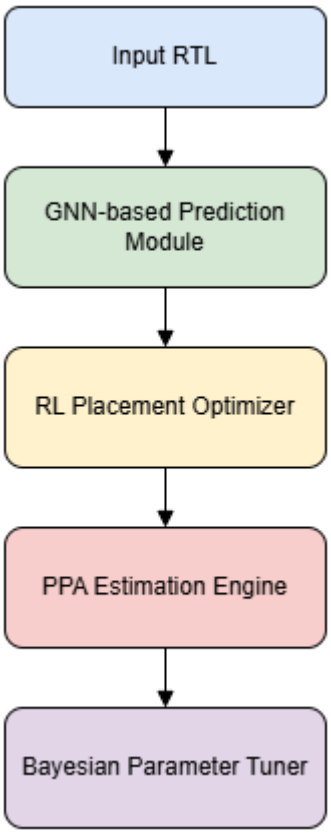

Figure 2: Diagram showing the structure of a cross-stage ML pipeline integrating reinforcement learning, GNNs, and parameter tuning for floorplanning decisions [3]

Figure 3 displays the correlation between predicted and actual power values, highlighting the accuracy of ML models in early-stage power estimation.

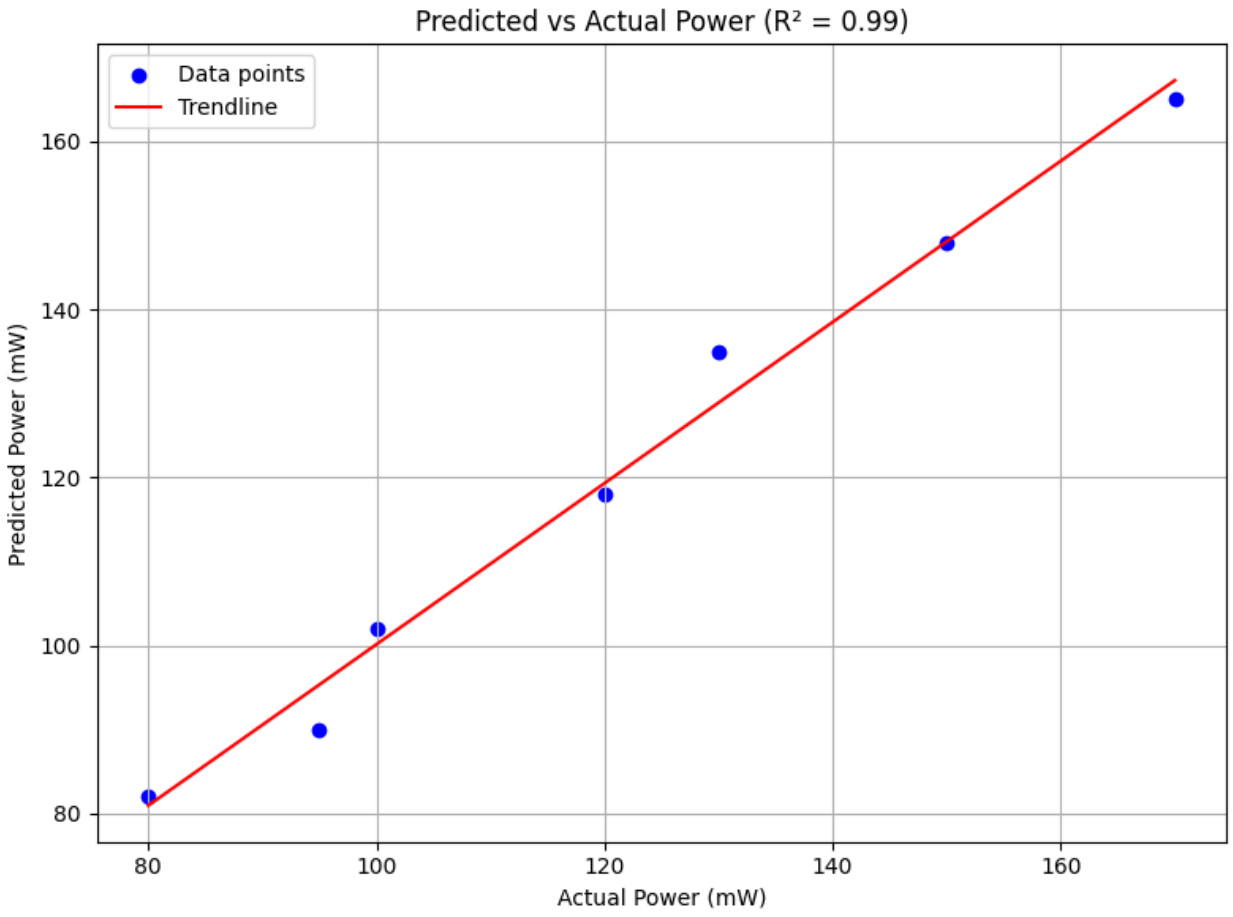

Figure 3: Graph showing predicted vs actual power values in ML-augmented early floorplanning systems [7]

Table 1: Comparative Overview of ML Techniques and Their Impact on PPA Metrics in Floorplanning

Reference	ML Approach	Target Stage	Key Metrics Improved	Reported Gains
[1]	Neural Networks	Logic Synthesis	Area, Timing	Moderate PPA gains with early predictions
[2]	Reinforcement Learning	Floorplanning	Wirelength, Power	Reduced iteration cycles
[3]	RL with Graph Encoding	Block Placement	Timing, Area	Improved convergence
[4]	Hybrid GNN and XGBoost	Cross-Stage	TNS, WNS, Power	~15–20% reduction in PPA violations
[5]	CNN-based Prediction	Early Placement	Power	High accuracy in early estimates
[6]	Graph Attention Networks	RTL-Level	Delay Paths	91% accurate delay predictions
[7]	GATs and Boolean Graphs	Logic Optimization	Area, Delay	Lower logic complexity, reduced runtime
[8]	End-to-End RL Framework			

7. Early RTL-Level Predictions and Timing Sensitivity

The key strength of the installation of machine learning on floorplanning is that it can be utilized to compute timing-restrictive paths in the RTL. To compute such paths in the classical EDA process, synthesis and placement runtime is needed, both of which are expensive to compute and time-consuming. To address such an issue, it has obtained machine learning models to achieve experience on the correlation between the attributes of the RTL code and post-placement reserve times.

The application of GAT models has achieved reasonable success in the learning of abstract syntax trees (ASTs) written in RTL. The path delays are also determined by the models, as well as the areas of the code that tend to create the worst-case slack infraction. It is explained by the fact that the designers are able to make modifications to the RTL implementations, and it can resynthesize the implementation again without high-impact engineering change orders later on in the flow. These experiments have suggested that more than 90 percent of prediction delay, when full layout information is unavailable, can be predicted [6].

What finer details can be examined with the help of the models include which logic blocks are the most prone to timing degradation, other than prediction. This knowledge can focus attention on the areas that need it most and emphasize the optimization activities. One of them will be the restructuring or the shift of the non-critical units concentrated in the high-fanout regions or high-load

regions. The consequent effect is that the design cycle is less unpredictable, more refined, with fewer surprises during the design stage, and fewer chances of failure during the later stage of its design [6].

8. Boolean Logic Optimization and Graph-Based ML Representations

It is optimized on logic synthesis and typically has undergone deterministic transformations, including De Morgan's laws, Karnaugh maps, and rule-based reduction schemes. These classical techniques, though, do not work in high-degree design cases where the truth tables and the Boolean representations are growing exponentially and the search space is essentially non-computable.

Machine learning can offer another logic of redressing the problem as merely a classification problem. Here, the logic expressions are converted to graphs, e.g., pairwise merged graphs, majority-inverter graphs, and ML classifiers (with special attention to the graph attention networks in specific cases) are trained to learn the most favorable implicants. These models will be inclined to capture the trends in the various designs of the logic that can be transferred to new functions with minimal or no retraining. These have been highly accurate in making small sets of logic phrases which maintain the actions of logic Ho, and at a much lower runtime burden [7].

These methods have provided a two-fold advantage in that, in addition to providing convergence expediency over the conventional synthesis products, they have also provided improved PPA through the elimination of additional logic in the initial design. In addition, the models can be applied as front-end logic optimizers which can be used prior to the mapping processes or the placement processes being implemented as part of the physical design processes, resulting in a smaller and more time-efficient netlist [7].

9. End-to-End ML Frameworks for Unified Chip Design

Practically, all the new developments have shifted towards end-to-end ML pipeline construction, with the prediction, placement, and optimization processes being within a single and closed solution. The designs combine reinforcement learning, deep neural networks, and Bayesian optimization with the design process of floorplanning and parameter tuning.

A pipeline in which reinforcement learning is applied to the first floorplan and block placement by learned policies is one of the architectures that can be applied. The forecasting of the performance, power, and location of the created floorplans with the assistance of deep neural networks, in turn, presupposes the nature of design benchmarks and data on the SoC. Lastly, Bayesian optimization is applied to optimize several design parameters of buffers, routing constraints, and power constraints in a bid to achieve an optimal trade-off of PPA and yield.

Such systems of integration tally with the scale standards within the industry in regard to scale, and experimental results of 7 nm and 5 nm node experiments show that the aggregate PPA has increased by 17.8 percent, and the time taken to close is reduced 21 to 25 times. In addition, the performance efficiency of these systems was achieved not only due to their functionality but also purposefully in the manufacturing since the quality of the yield prediction was as high as 92.6 percent [8].

It is being used with the feature engineering of functions, i.e., the high-dimensional input space is reduced with the help of principal component analysis (PCA) and manual techniques. This is because it would be easier to generalize the performance of the models, and the critical timing or physical features of the design would not be missed. This type of sophisticated system shall become the future trend in incorporating ML-EDA into design, forecasting, and amendment integrated into one intelligent system [8].

10. Emerging Trends and Future Prospects

The expansion that is accompanied by ML models may only increase the accuracy of the initial forecast as new datasets are received. Reinforcement learning agents, parameterized dynamically on their reward capabilities and silicon validation feedback, can be used to optimize future designs and hence can provide a closed-loop design and post-silicon tuning learning system.

Moreover, the further development of graph neural networks (specifically, the attention-based and transformer models) can also ensure that the description of the practical and logical relationships between the chips will be more efficient. In addition to that, the amalgamation of the mind could soon be provided to us as the novelty of multimodal learning rises and the textual, physical, and logical specifications are merged. It can result in a more natural and higher-order interaction between design tools, machine inference, and human intent interacting in a synergistic manner.

Another trend is the method of designing that is becoming more popular nowadays. Although this review has concentrated on the prediction and optimization focus, it may be the case that in the future systems will be capable of constructing completely different RTL code or floorplan architecture from abstract performance requirements. These technologies would then cause the human designer to become the overseer who delegates to the automated system the task of producing the optimized chip design.

The issue is the question of interoperability. The existing ML-based tools can be sold as independent entities or as tailor-made data interfaces that might be modeled alongside the existing EDA procedures. They will need such interfaces to be standardized and will be compelled to inject them directly into commercial toolchains to enable them to be more widely embraced by the industry.

The establishment of academic and industrial databases, labeled netlists, and floorplan outcomes will grow and will consequently make cross-referencing and comparing the use of ML models a more challenging undertaking. This will assist in the setting up of best practices and reproducibility, which has been an issue with some of the initial reinforcement learning-based placement studies.

11. Conclusion

The use of machine learning in the earlier phases of chip design has radically changed the stage of the floorplanning process in power, performance, and area prediction. ML models may show the worth of the estimation that may render the design choices more efficient and more accurate via logic synthesis, after which block placement and parameter optimization take place. The following enhancements are able to detect bottlenecks sooner, approximate the post-layout measures, and perform adaptive optimization without, literally, running a protracted simulation or creating a synthesizing workflow.

The sources utilized in this review give a person another picture of this change. With the general literature trend pointing to predictive and autonomous design flow, there is a tendency to expand to end-to-end reinforcement learning systems with logic synthesis in the form of neural networks, as the overall literature has demonstrated. Graph representations, RTL timing path optimization, as well as machine-learned Boolean logic optimization are other optimizations of this new field.

Since EDA will be left on the periphery of AI, the systems will be more confined to such features as generalization, real-time feedback, and cross-stage intelligence. These properties will not only enable the chip design process to be faster, but also will enhance yield as well as reliability in high-level process nodes. Machine learning and floorplanning is a significant undertaking towards self-optimizing design systems that are more extensible, intelligent, and more reflective of current silicon requirements.

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