Design Low Power CMOS D-Flip Flop usingModified SVL Techniques

Madhu Shakya
M-Tech VLSI Design
SRCEM
Gwalior (M.P) INDIA

Shweta Agrawal
Assistant Professor, Dept. Electronics
& Communication Engineering
SRCEM
Gwalior (M.P), INDIA

Abstract

In this paper high recital CMOS D-flip flop circuit has proposed, which is comprehensively used in analog and digital systems. CMOS D flip flops are first preference to implement different type of binary counters, shift registers and analog and digital circuit system. In CMOS technology leakage power is primary significance. Toreduce power dissipation and to develop the time of battery backup,the supply voltage to the given circuit during standby modeshould be reduced.Modified SVL technique is applied to CMOS D flip flop circuit,which employs in order to suppression of signals and reduce powerdissipationdue to leakage currents in reserve form. Also theproposed design uses less number of clocked transistors, thusreduces the dynamic power consumption as well as leakage current to accessible design. Each accessible design and proposed design is replicated utilizing Cadence device at 90nm and 45nm technology.

Key Words:CMOS, D-Flip Flop, Leakage Power, Leakage Current, Delay, Cadence.

1. Introduction

Bi-stable devices (popularly called Flip-flops) are mostly utilized as solitary bit memory cells. Flip flop have each of two steady condition, logic 1 or logic 0. [1]We need totrigger the flip flop to get in to any one of two stable states byapplying an external pulse as input. The output remains which steady condition until other pulse is utilized to modify to condition. Wecan also modify the flip flop output by applying proper inputsother than trigger. Flip flops are widely used in most sequentialcircuits like counters, shift registers etc…Delay flip flop [2]stores whatever the input bit pattern applied at its D input.This feature helps in processing of data bit by bit by other partsof the digital circuit to get solutions for complex functions. Gate level diagram positive edge triggered D type flip flop is given in Fig.1. The major drawback of the Set Reset flip flop(i.e. its undeterminable output and if S=R=1) is conquer through the D flip-flop. D flip-flop, given in Fig.1 known as Data flip-flop since its capability to 'latch' and store data, or Delay flip-flop because latching and accumulate data is utilize to make a impediment in the processing of that data through acircuit.

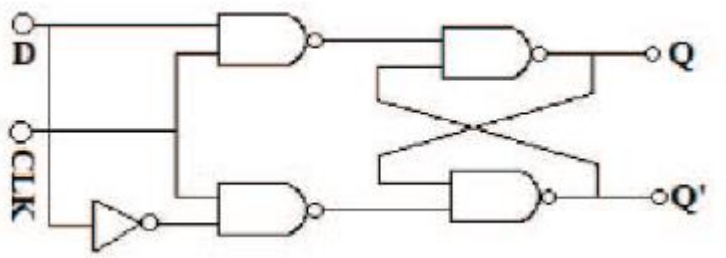

Fig.1 Gate level diagram of D type flip flop

The simplest form of a D Type flip flop [3] is a highactivated SR type along with an inverter so that theS=R=1(which leads to uncertain output) input mixture have circumvent. This alteration prevents each the undetermined as well as non-allowed condition represents in the SRflip-flop. In D flip flop, S and R inputs, are replaced by asingle D input which simply transfers the input bit to outputwith some delay in the presence of a clock pulse.

2. CMOS D-Flip flop Architecture

Flip-flops are the essential structure block of the digital electronics systems utilized within mainframe and most of several kinds of systems. Flip flop are electronic device that provisions position information. The D flip flop output pursue the input which provide the output as input.D signify “DATA” it accumulate the value which is on the data line. Flip-Flop is an electronic circuit which stores the rational condition of individual or extra data input signal are answer to the clock pulse. This D flip flop have set or reset during inverter circuit. There are two kind of flip flop solitary is single edge triggered (SET) and other solitary is double edge triggered (DET). Single edge triggered flip flop is straightforward and simple to propose as works on each increasing or diminishing edge of a clock. The architect of TSPC D flip-flop by 5 transistors is given at this time. The graphic of 5 transistors TSPC D flip-flop is given in Fig.2. This flip-flop is constructs utilized 3NMOS and 2 PMOS transistors. This edge triggered flip-flop is diminutive in region because it demonstrates low transistor count merely 5 transistors are utilized and it besides decrease power consumption. In 5T TSPC DFlip Flop, TSPC stands for True Single Phase Clocked logic TSPC circuit method utilized include single phase of the clock and evade skew troubles thus developing the performance of a digital system.These exclusion of skew involve considerable reserves in fragment region and power consumption [3]. Figure:2 given the graphic of 5T TSPC D FlipFlop. [4, 5]
While CLK and input D each are grow then the transistors P1, N3 are OFF and residual transistors P2, N1, N2 are ON. The output turn elevated. Even as in ON clock period suchlike is the worth of input that turn output.

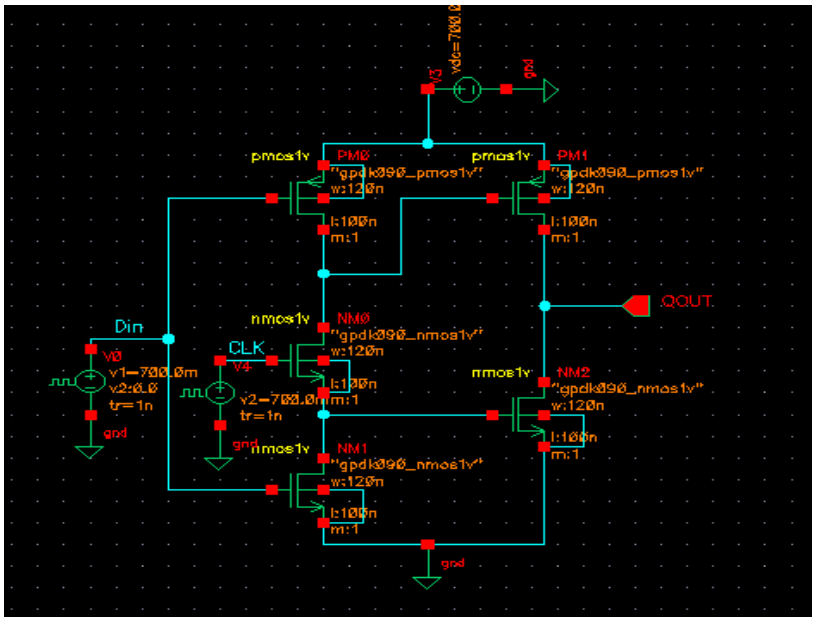

Fig.2 CMOS D-Flip Flop

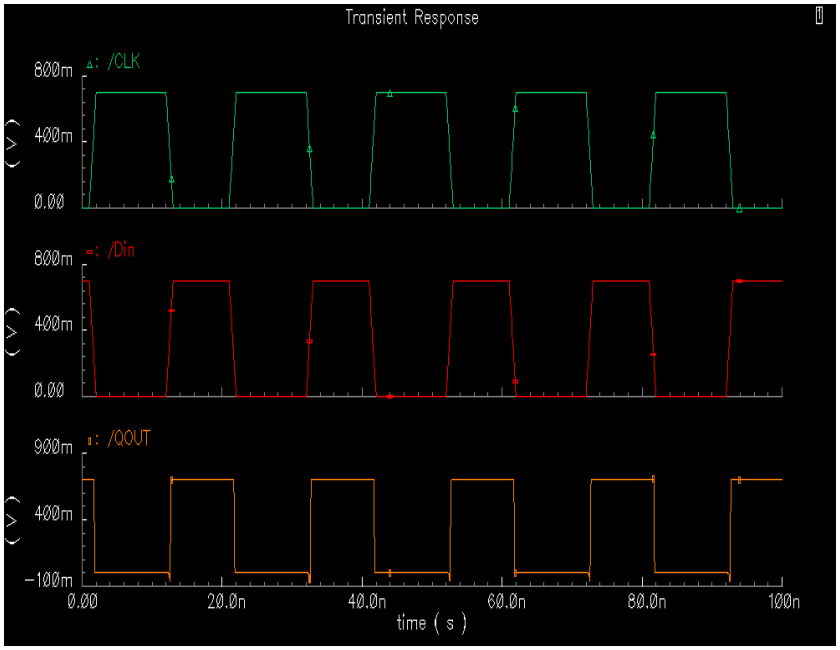

Fig.3Transient Response of CMOS D-Flip Flop

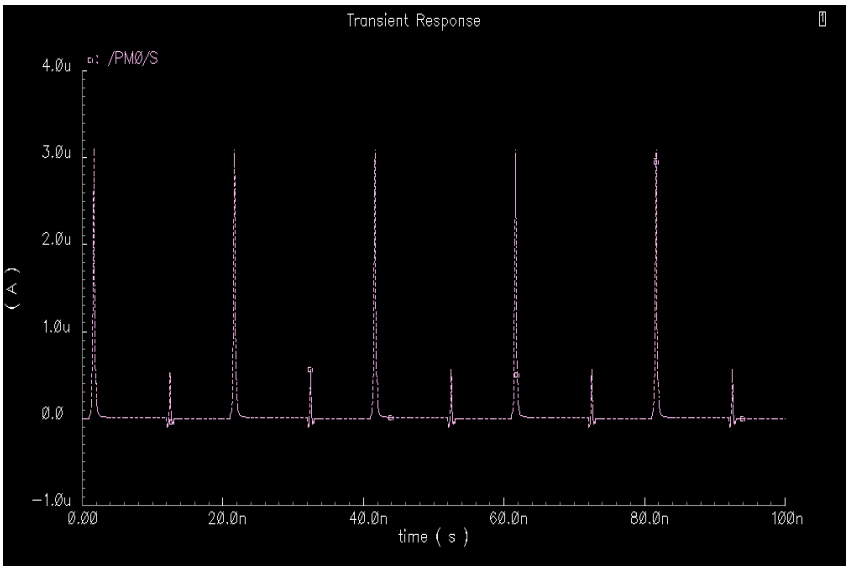

Fig.4Leakage Current of CMOS D-Flip Flop

3. Leakage Reduction Techniques Applied On CMOS D-Flip Flop

I. SVL Technique applied on CMOS D-Flip Flop

SVL is the acronym for Self Voltage Level. SVLtechnique is used to reduce leakage power [6] in clockedsystems like flip flops during standby mode of operation i.e when clock=0.SVL method utilize PMOS and NMOS transistor in equivalent as pull up network or pull down system. Pull up transistors gate isconnected with complement of clock signal and pull downtransistors gate terminal is connected with clock .This technique to reduce leakage [7] power uses a clock signal asthe control signal to control supply voltage to D flip flop.Hence the name self voltage level is justified. When clock = 1, clock bar=0 and Psw1 will becomeON, Nsw1 will be in off state. Clocked circuit will be connected to Vdd.

When clock =0, the circuit is in standbymode and do not require more power supply to maintain instandby mode. Hence even if we reduce the supply voltageduring standby mode it will work perfectly fine and powerconsumption will be reduced, especially the leakage power thatflows when transistors are in off state will be reduced.When clock = 0, Nsw2 is OFF.PMOS transistorprovides bad logic ‘0’ i.e it provides Vth at output when usedas pull down. Since Psw2 is PMOS transistor connected as pulldown instead of ground it will provide some finite voltage atthe node “virtual ground”. This virtual ground is associated to supply terminal of the drag downward NMOS transistors of regulator circuit. If slightly positive voltage is applied to source of NMOS transistors its leakage current will be reduced instandby mode. Similarly at the pull up side Psw1 is OFF andNsw1 is ON but provides bad logic ‘1’ since it is used pull up.Clocked circuit will be connected with a virtual supply [1]voltage which is less than Vdd. Thus during standby mode (i.ewhen clock = 0) the clocked circuit leakage power is reduced.

The following Fig. 3 shows the D flip flop designusing SVL technique. The D flip flop is implemented usingfive transistors, two PMOS (P1 and P2) and three NMOStransistors (N1,N2 and N3).

Case1: clock = 1(active mode)

Psw1 is ON, Nsw2 is ON,Psw2 is OFF ,Nsw1 isOFF. D flip flop is connected to Vdd and ground for normalcircuit operation.

If D_in=0, P1,N1,N3 are ON and P2,N2 are OFF, connectingQ to ground i.e Q = 0

If D_in=1, P1, N3 are in OFF state and N1,N2,P2 are in ONstate , connecting Q to Vddi.e Q = 1

Case2: clock = 0(standby mode)

Psw1, Nsw2 are in OFF state i.e open circuits. Nsw1is ON but as it is used as pull up it provides Vdd-Vth as thesupply voltage for D flip flop. The drop is due to resistivenature of NMOS when used as pull up. Similarly, Psw2 is ONbut as it is used as pull down it provides finite positive voltageinstead of ground (0 volts).This virtual ground positive voltageslightly reverse biases the NMOS transistors of D flip flop andreduces leakage power in standby mode. D flip flop's PMOStransistors leakage power [8] is reduced, since they areconnected to virtual supply in standby mode.

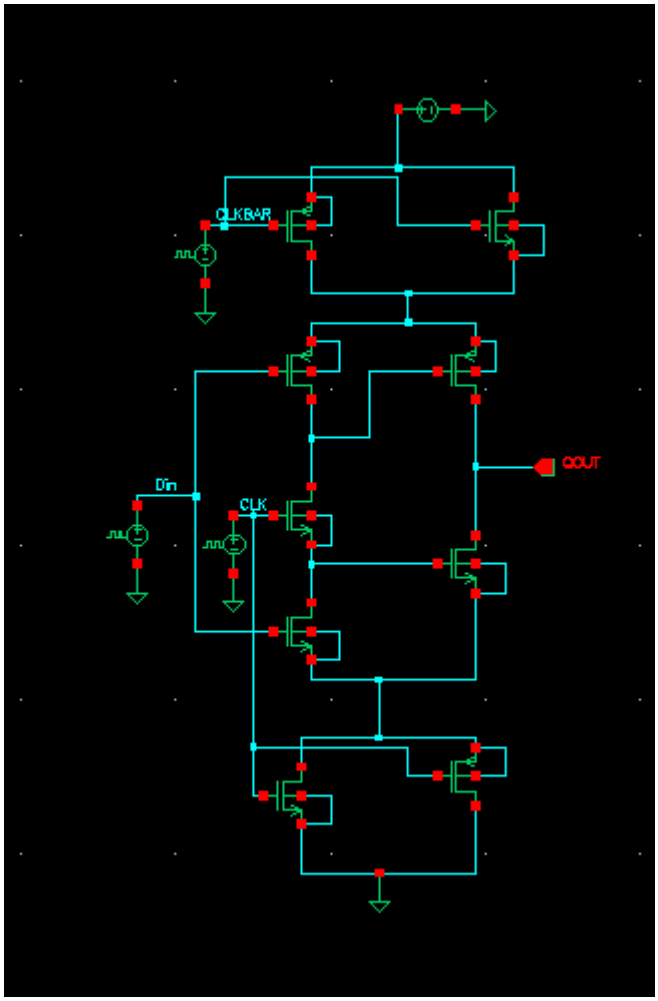

Figure.5 Schematic of CMOSD-Flip Flop with SVL

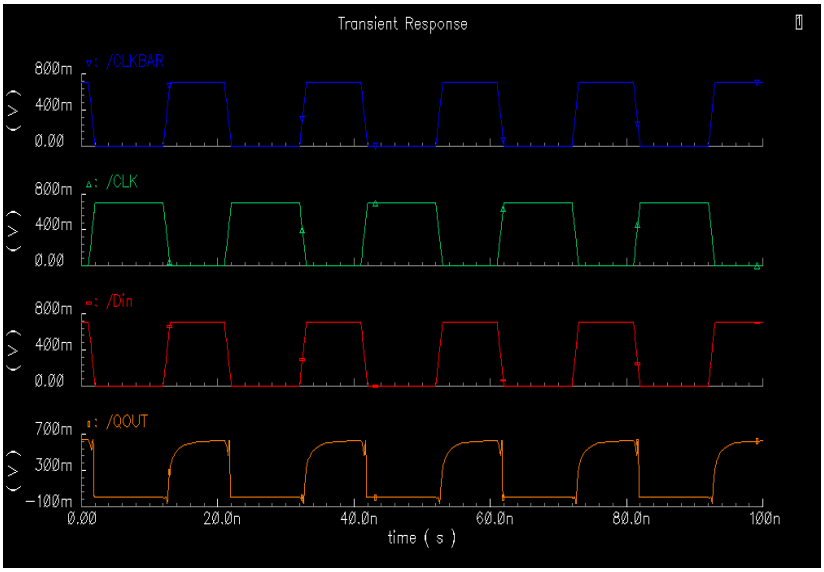

Fig.6Transient Response of CMOS D-Flip Flop with SVL

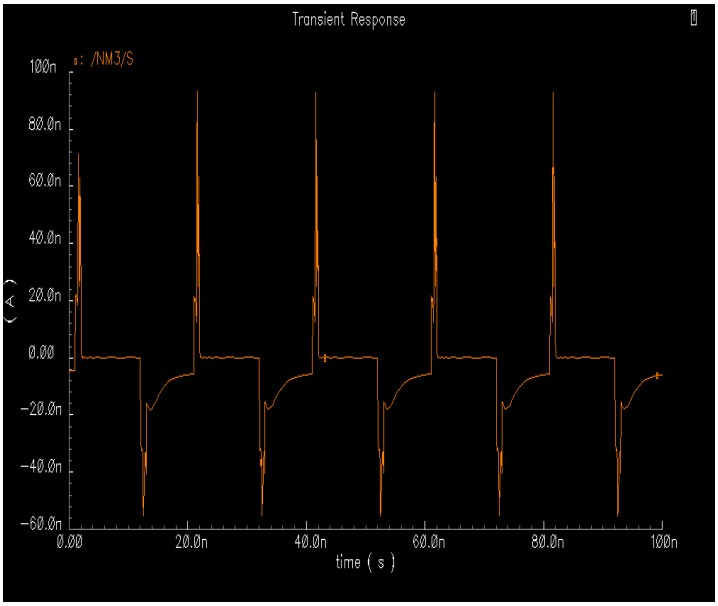

Fig.7Leakage Current of CMOS D-Flip Flop with SVL

II. Modified SVL Technique applied on CMOS D-Flip Flop

The following Fig. 6 shows the Delay flip flop design using Improved SVL technique. The D type flip flop isimplemented by using five transistors, two PMOS (P1 and P2)and three NMOS transistors (N1, N2 and N3).

Case1: clock = 1(active mode)

Psw1 is ON, Nsw2 is ON,Psw2,Psw3 are OFF,Nsw1,Nsw2 are OFF. D flip flop is connected to Vdd andground for normal circuit operation.

If D_in=0, P1,N1,N3 are ON and P2,N2 are OFF, connectingQ to ground i. e Q = 0

If D_in=1, P1, N3 are in OFF state and N1,N2 and P2 are inON state, connecting Q to Vddi. e Q = 1

Case2: clock = 0(standby mode)

Psw1, Nsw3 are in OFF state i.e open circuits. Nsw1,Nsw2 are ON but as they are used as pull up they provide Vdd-Vth as the supply voltage for D flip flop. During stack of two NMOS transistors associate threshold leakage current is condensed. Similarly Psw2, Psw3 are ON but as they are used as pulldown they provide finite positive voltage instead of ground (0volts).This virtual ground positive voltage slightly reversebiases the NMOS transistors of D flip flop and reduces leakagepower [8] in standby mode. For PMOS transistors of D flipflop leakage power is reduced, since they are connected tovirtual supply in standby mode.In Improved SVL Technique in addition to reductionof supply voltage, leakage current flow is reduced by the use ofstacked [7] NMOS transistors. Hence supply power providedto the basic flip flop circuit is significantly reduced in staticmode. Because leakage power consumption in stationary state is straightly proportional to the supply voltage and current, therefore leakage power is condensed in reserve form utilized Improved SVL Technique.In addition to leakage power reduction in ourproposed design we also reduced no. of clocked [9] transistorswhich helps in speeding up the operation of the circuit and alsocontributes a little in reducing dynamic power consumptionalso. Though we have used this technique for D Flip Flop it'sobvious that we can use technique for any clocked circuit toreduce leakage power in static mode.

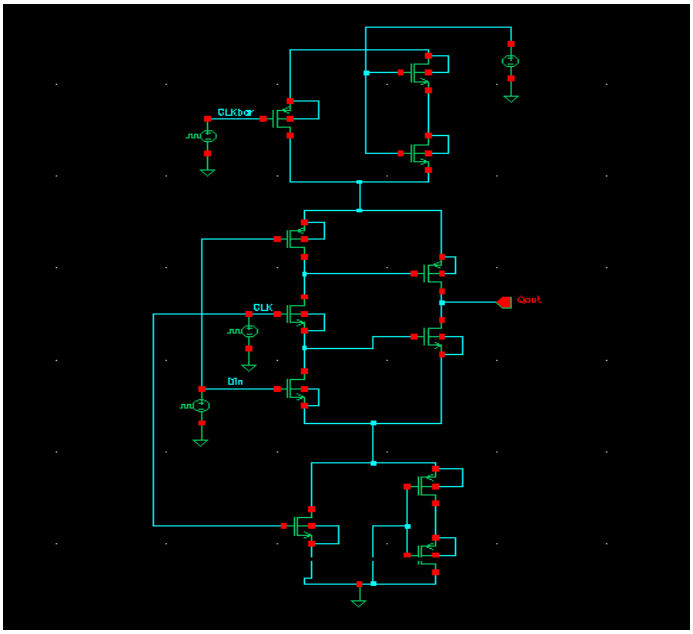

Figure.8 Schematic of CMOSD-Flip Flop with Modified SVL

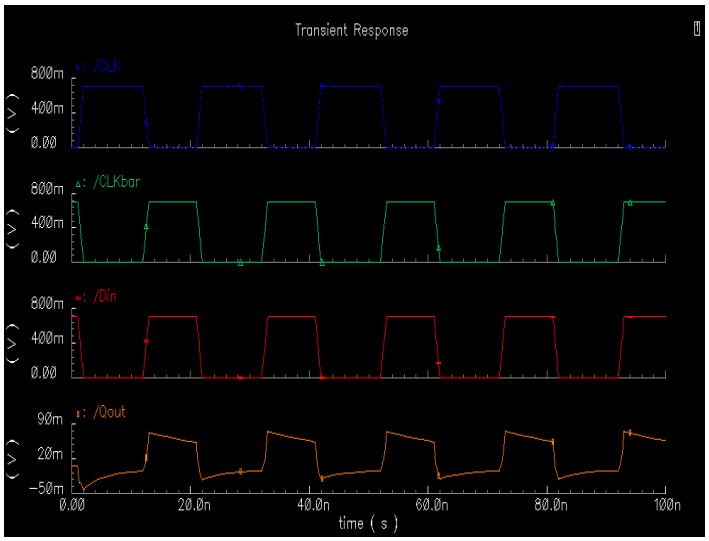

Fig.6Transient Response of CMOS D-Flip Flop with Modified SVL

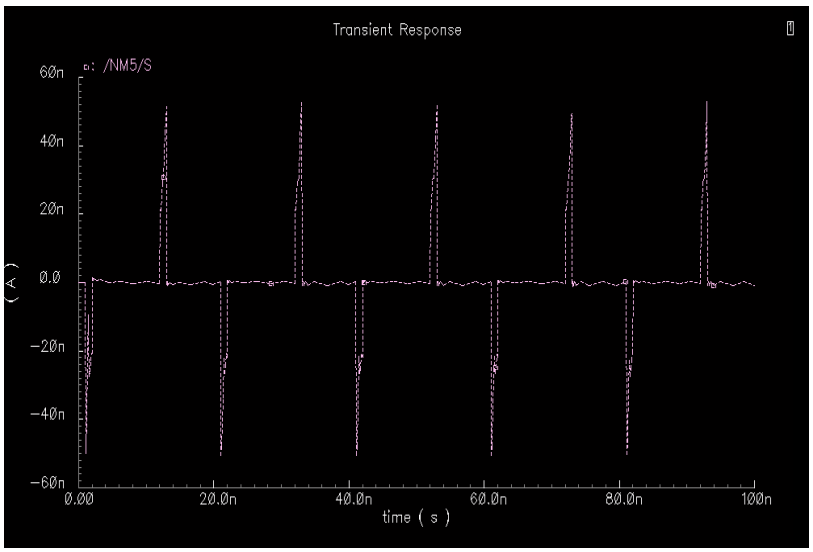

Fig.10Leakage Current of CMOS D-Flip Flop with Modified SVL

4. Simulation Result

CMOS D-Flip FlopSimulation has been done on cadence tool using the 90nm and 45nm technology with a nominal supply voltage Vdd= 0.7 V. The gate leakage being the only dominant mechanismat room temperature 27°C, different techniques have used forreduction of power consumption and maintaining theperformance of CMOS D-Flip Flop, Modified SVL method suppresses themaximum total leakage in comparison to SVL technique, it improve the parameter like Leakage Current or power, and Propagation impediment.

A. Leakage Power Analysis

When we reduce the channel length or provide scaling sothe leakage power is increase, Leakage power providesstandby power of any device. Leakage power association to CMOS D-Flip Flop among SVL and customized SVL is given in beneath Fig. Leakage current may be occurs from substrate injection belongings and sub-threshold voltage. Leakagepower is wastage of power supply and leakage power ofSchmitt trigger is :

$$P_{LEAK} = I_{LEAK} V_{dd}$$

Where P_{LEAK} is leakage power of CMOS D-Flip Flop, I_{LEAK} abbreviated for leakage current, Vdd is power supply.

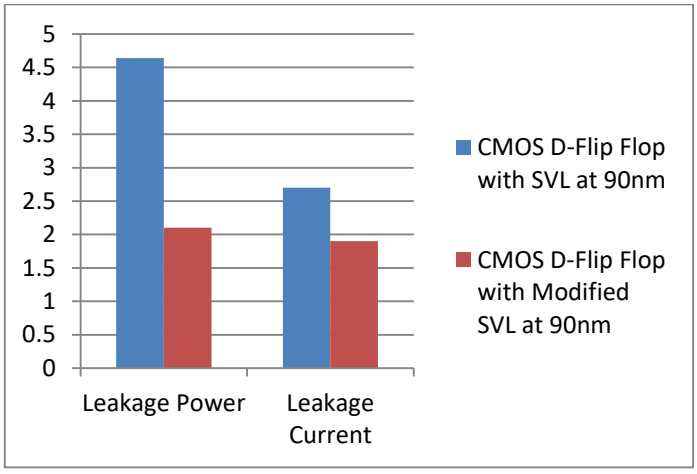

Fig.11 Comparison Graph of CMOS D-Flip Flop at 90nm

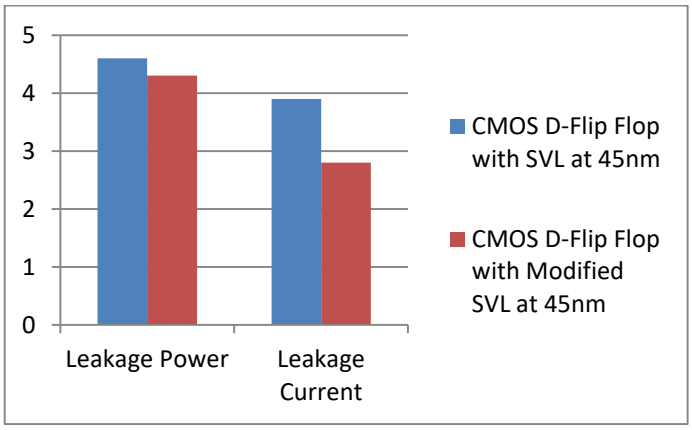

Fig.11 Comparison Graph of CMOS D-Flip Flop at 45nm

B. Propagation Delay

CMOS D-Flip Flop is used in place of buffer and reduce delayas well as power consumption. The most positivecharacteristic of CMOS D-Flip Flopis its adjustable thresholdvoltage, and it can be controlled, the threshold voltage can bechosen to be above or below, a voltage at which bufferusually operates. Therefore a CMOS D-Flip Flopcan bedesigned to switch faster than a buffer leading to a reductionin delay, the adjustable low-voltage threshold of the CMOS D-Flip Flop maneuver extra noise and voltage anomaly as evaluate to buffer. The time in use for a CMOS D-Flip Floplogic gateoutput to change after one or more inputs have changed isknown as propagation delay.

The simulation Results examine that Modified SVL with CMOS D-Flip Flopgives a better performance as compared to SVL techniques and less delay in 90nmand 45nm technology at supply voltage 0.7 V. The Delay of the through during a signal transition is given as:

$$Delay = 0.69R_{eq} \times C_L$$

Where in equationis the R_{eq} resistance that isimplemented using the feed through cell and $C_L$is the loadcapacitance.

Comparisons Result Summary of Technique applied on CMOS D-Flip Flopon the basis of different supply voltageis shown below table 1.

Table 1 Simulated Result Summary

Performance Parameter	CMOS D-Flip Flop	CMOS D-Flip Flopwith SVL	CMOS D-Flip Flopwith Modified SVL	CMOS D-Flip Flop	CMOS D-Flip Flop with SVL	CMOS D-Flip Flopwith Modified SVL
Technology Used	90nm	90nm	90nm	45nm	45nm	45nm
Supply Voltage	0.7V	0.7V	0.7V	0.7V	0.7V	0.7V
Leakage Power	4.8µW	4.64nW	2.1nW	6.3nW	4.6pW	4.3pW
Leakage Current	3.6µA	2.7nA	1.9nA	4.5nA	3.9pA	2.8pA
Propagation Delay	22µs	84ns	69ns	66ns	98ps	82ps

Conclusion

CMOSD-Flip Flophas low power requirement of VLSItechnology for battery operated circuits power reduction isimportant key factor, so we are configured low power high performance CMOS D-Flip Flopwith SVL and Modified SVL techniques for enhancing the circuit parameter such as leakage power, Current and Propagation interruption. Toreduce power dissipation and to develop the time of battery backup,the supply voltage to the given circuit during standby mode should be reduced.Modified SVL technique is applied to CMOS D flip flop circuit, which employs in order to suppression of signals and reduce power dissipation due to leakage currents in

reserve form. Also theproposed design uses less number of clocked transistors, thusreduces the dynamic power consumption as well as leakage current to accessible design. In this paper comparative description of SVL and Modified SVL techniques havebeen offered on the bases of min leakage power at supply voltage Vdd=0.7 V, threshold voltage(0.35 V) and input control voltage is also 0.7V.Simulation result provides CMOS D-Flip Flopwith Modified SVL techniques is better than SVL techniques. This kind of CMOS D-Flip Flop design is utilized in less power statement structure.

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