IJRAR.ORG E-ISSN: 2348-1269, P-ISSN: 2349-5138

INTERNATIONAL JOURNAL OF RESEARCH AND ANALYTICAL REVIEWS (IJRAR) | IJRAR.ORG

An International Open Access, Peer-reviewed, Refereed Journal

LOW POWER OPTIMIZATION 8T FULL ADDER USING FINFET TECHNOLOGY

[1]R. Gopichand,[1]P. Sowjanya,[1]M. Lakshmi Jahnavi,[1]M. B.S Srimannarayana, K.Siva Ranjani[2], Kondamuri Purna Sidhu, [2]

[1]U.G. Scholar, Department of Electronics and Communication Engineering, Bonam Venkata Chalamayya Engineering College (Autonomous), Odalarevu, Andhra Pradesh, India.

[2] Assistant Professor, Department of Electronics and Communication Engineering, Bonam Venkata Chalamayya Engineering College (Autonomous), Odalarevu, Andhra Pradesh, India.

Abstract: The continuous advancement of portable and battery-powered electronic devices has increased the demand for low-power VLSI circuit design. Among various digital building blocks, the full adder plays a vital role in arithmetic units such as multipliers, processors, and digital signal processing systems. Therefore, optimizing the power consumption and performance of full adder circuits is an important research objective. In this paper, a low-power 8-transistor (8T) full adder based on FinFET technology is proposed. FinFET devices offer superior electrostatic control over the channel, effectively reducing short channel effects and leakage currents compared to conventional CMOS technology. The proposed design minimizes the transistor count while maintaining reliable logic operation and improved switching performance. The circuit is designed and simulated using the Cadence/HSPICE environment with nanoscale FinFET technology. Simulation results demonstrate that the proposed 8T full adder achieves reduced power consumption, lower propagation delay, and an improved power-delay product when compared with conventional CMOS-based full adder designs. The proposed architecture is therefore suitable for low-power and high-performance VLSI applications.

Keywords: FinFET Technology, Low Power VLSI, 8T Full Adder, Power Delay Product, Nano-scale Integrated Circuits.

I .INTRODUCTION

The rapid advancement of Very Large Scale Integration (VLSI) technology has enabled the development of highly complex and compact digital systems. As the demand for portable and battery-powered electronic devices continues to grow, reducing power consumption has become a major challenge in modern integrated circuit design. In nanoscale technologies, traditional Complementary Metal–Oxide–Semiconductor (CMOS) devices suffer from several limitations such as increased leakage currents, short-channel effects, and higher static power dissipation. These issues significantly affect the performance, reliability, and energy efficiency of digital circuits.To address these challenges, Fin Field Effect Transistor (FinFET) technology has emerged as a promising alternative to conventional CMOS technology. FinFET devices employ a three-dimensional fin-shaped channel structure that provides better electrostatic control over the channel region. This structure effectively reduces leakage currents, suppresses short-channel effects, and improves switching performance. Due to these advantages, FinFET technology has become widely adopted in modern semiconductor manufacturing for designing low-power and high-performance integrated circuits.Among the various components used in digital systems, the full adder is one of the most fundamental building blocks in arithmetic circuits. Full adders are extensively used in applications such as microprocessors, arithmetic logic units (ALUs), digital signal processors (DSPs), and multipliers. Since

addition is one of the most frequently executed operations in digital computing, the efficiency of a full adder significantly impacts the overall performance and power consumption of a system. Therefore, designing full adders with low power consumption, reduced delay, and minimal transistor count has become an important research area in VLSI circuit design.In recent years, several full adder architectures have been proposed using different logic styles and transistor configurations. However, many conventional designs require a large number of transistors, which leads to increased power consumption and larger chip area. To overcome these limitations, compact designs such as 8-transistor (8T) full adders have gained attention due to their reduced complexity and improved energy efficiency.

In this paper, a low-power 8T full adder using FinFET technology is proposed to achieve improved performance and reduced power consumption. The proposed design focuses on minimizing transistor count while maintaining reliable logic operation and high-speed performance. The circuit is implemented and simulated using appropriate VLSI design tools to evaluate its power consumption, delay, and power-delay product. The results demonstrate that the proposed FinFET-based full adder provides improved efficiency compared to conventional CMOS-based adder designs, making it suitable for low-power and high-performance VLSI applications.

II. LITERATURE SURVEY

The full adder is one of the most fundamental building blocks in digital arithmetic circuits such as arithmetic logic units (ALUs), microprocessors, multipliers, and digital signal processors. Since addition is a frequently performed operation in digital systems, the design of efficient full adders plays a critical role in determining the overall performance, power consumption, and area of VLSI systems. Consequently, extensive research has been conducted to design high-speed and low-power full adder circuits.

Early full adder implementations were primarily based on conventional CMOS logic styles. Shams et al. analyzed the performance of different CMOS full adder cells and showed that traditional designs typically require a large number of transistors, which results in higher power consumption and larger silicon area [6]. As technology scales to nanometer dimensions, these CMOS-based circuits also suffer from increased leakage currents and short-channel effects. To overcome these limitations, several researchers proposed alternative full adder architectures using different logic styles. Jiang et al. introduced a multiplexer-based low-power full adder that significantly reduces transistor count while maintaining acceptable performance [11]. Similarly, Zimmermann and Fichtner compared CMOS logic with pass-transistor logic and demonstrated that pass-transistor based designs can reduce capacitance and power dissipation, thereby improving energy efficiency [14].That logic circuits designed using FinFET technology exhibit improved switching performance and reduced power consumption compared to conventional CMOS circuits [7]. Due to their three-dimensional gate structure, FinFET devices offer better control over the channel region, which helps in minimizing short-channel effects and improving energy efficiency. Fossum and Trivedi also discussed the advantages of ultra-thin-body MOSFETs and FinFET devices for nanoscale integrated circuit design [9].

Therefore, designing compact and energy-efficient full adder circuits using FinFET technology has become an important research direction. In this work, a low-power 8-transistor full adder based on FinFET technology is proposed to achieve reduced power consumption and improved energy efficiency while maintaining reliable logic operation and acceptable delay performance.

III. PROPOSED SYSTEM

A.FinFET Technology Overview

The Fin Field-Effect Transistor (FinFET) is a three-dimensional transistor structure that overcomes the limitations of planar CMOS devices at deep-submicron technology nodes. The conducting channel is a vertical fin with a gate wrapping around three sides, offering superior electrostatic control and reduced short-channel effects (SCEs). FinFETs are particularly suitable for low-power, high-performance applications at 7 nm technology nodes and below .

FinFETs can operate in tied-gate or independent-gate (INDEP) configurations. INDEP mode allows dynamic threshold voltage adjustment, reducing leakage in standby mode while maintaining fast switching in active mode. This dual-mode operation enhances energy efficiency, noise immunity, and reliability, which is critical for IoT devices and battery-powered systems.

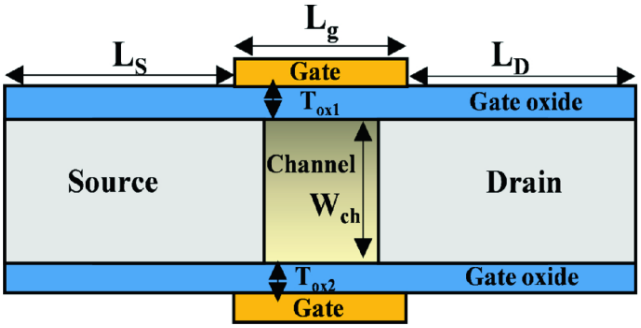
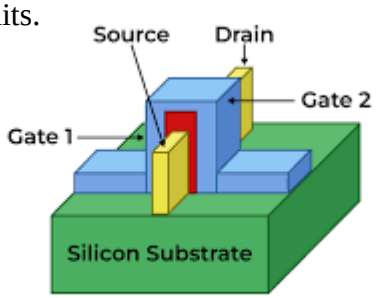


Figure 1 : Symbol of Double-Gate FinFET

B. Construction and Schematic of FinFET

FinFETs are fabricated with vertical fins on SOI wafers, where the fin height and width determine the effective channel width. A wraparound metal gate insulated by a thin oxide layer surrounds the fin, providing excellent gate control, reduced leakage, and high transistor density.

Advanced lithography and etching techniques allow high aspect-ratio fins, compact layouts, and integration into high-density circuits.



Structure of FinFET

The FinFET schematic shows the 3D nature of the device. The gate wraps around the conduction channel, significantly reducing parasitic capacitance and enabling low-voltage operation.

C.Design of FinFET-Based Full Adders

i. FinFET 10T Full Adder

The 10-transistor (10T) full adder is a low-power arithmetic circuit suitable for microprocessors, DSPs, and ALUs. Traditional CMOS 10T designs face high leakage, short-channel effects, and power dissipation at sub-22 nm nodes. FinFET 10T designs improve switching speed, reduce leakage, and enhance the power-delay product (PDP). These circuits use pass-transistor logic (PTL) combined with the superior gate control of FinFETs to achieve energy efficiency.

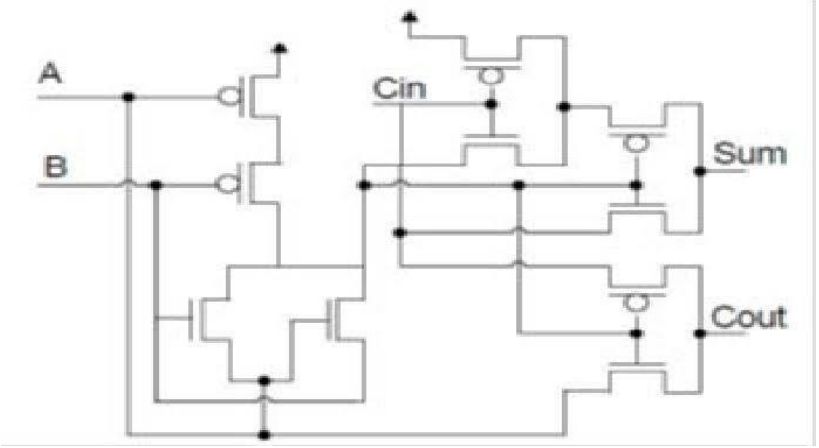


Figure 2: FinFET 10T Full Adder Schematic

ii. Proposed FinFET 8T Full Adder

The 8-transistor (8T) full adder further reduces the transistor count, resulting in a smaller chip area and lower power consumption, while maintaining high-speed operation. The 8T design is particularly effective for portable and IoT devices.

Key advantages:
Reduced dynamic and static power
Improved propagation delay
Smaller silicon footprint
High energy efficiency

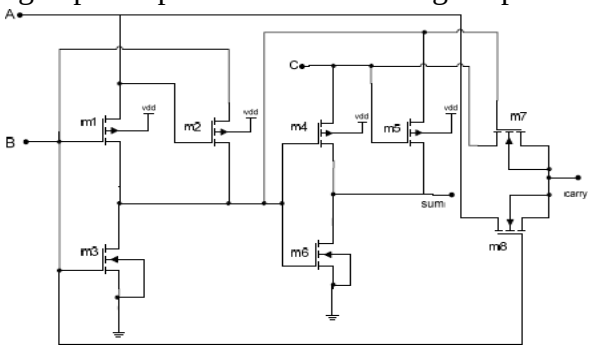


Figure3 : FinFET 8T Full Adder Schematic

IV.RESULT ANALYSIS

A.Schematic design of 8T Full Adder using FinFET

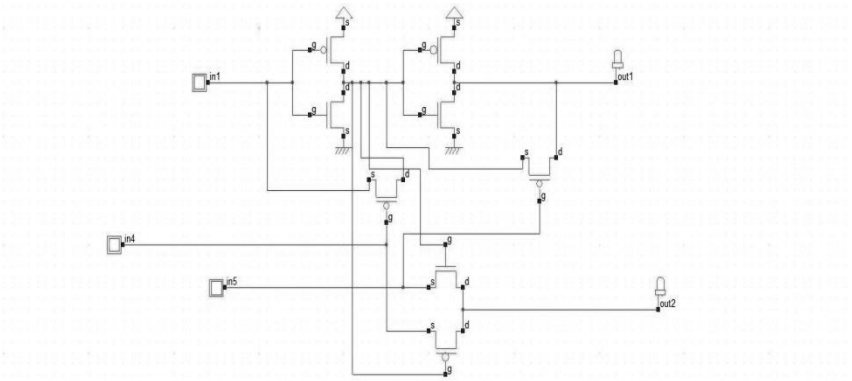


Figure 4: Schematic design of 8T Full Adder using FinFET

B.Layout of design of 8t full adder using FinFET

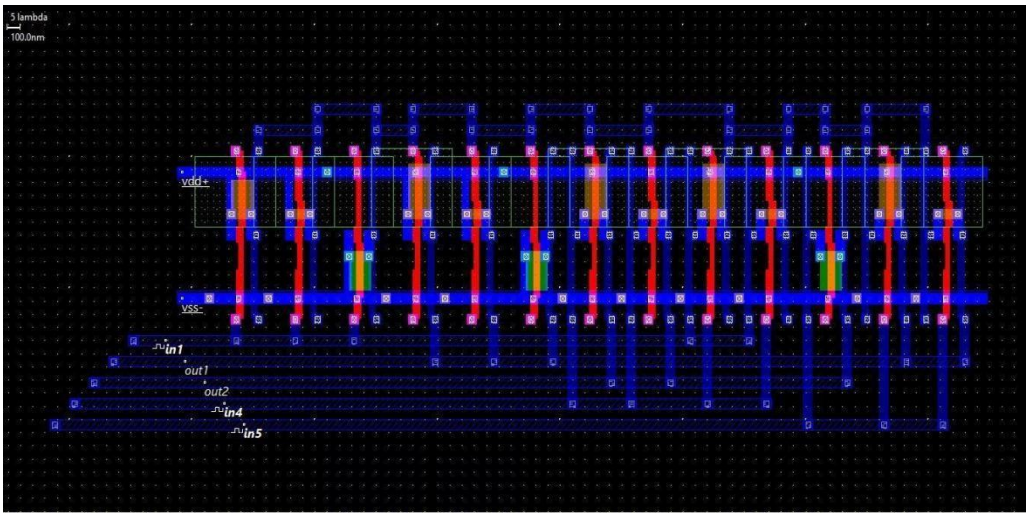


Figure5: Layout design of 8T Full Adder using FinFET

C.Simulation results of 8T Full Adder using FinFET

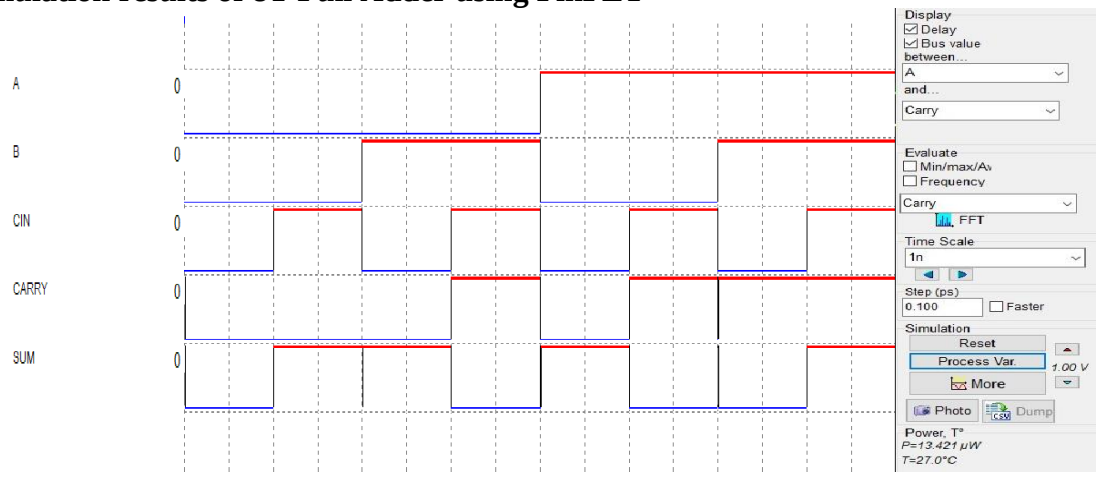


Figure6 :Simulation results of 8T Full Adder using FinFET

D. Comparison Table

Technology	Method	Power	Area	Delay	Number Of Transistors
FinFET 35nm	FinFET 8T Full Adder	13.421µW	18.9µm2	53.3ps	8
FinFET 35nm	FinFET 10T Full Adder	33.631µW	24.1µm2	16.8ps	10

Table: 1 Comparison Table

V. CONCLUSION

The proposed FinFET-based 10T and 8T full adders demonstrate significant improvements in power efficiency, speed, and reliability compared to conventional CMOS designs. The 10T full adder offers a robust balance of low power, high speed, and strong logic levels, making it suitable for high-performance and scalable VLSI systems. The 8T design achieves ultra-low power and compact layout, ideal for energy-critical applications. Overall, FinFET technology enables low-power, high-density, and high-speed arithmetic circuits, making these designs promising candidates for next-generation VLSI and portable electronic devices.

VI. Advantages

- Low power consumption
- High speed
- Compact layout
- Enhanced reliability
- Scalability to advanced nodes
- Flexible design trade-off

VII. Applications

- Portable and battery-powered devices
- Microprocessors and ALUs
- Digital signal processors (DSPs)
- Energy-efficient VLSI systems
- High-density integrated circuits

REFERENCES

[1] Ruchi Dantre and Sudha Yadav, "Design and analysis of FinFET based high performance 1-bit half adder–half subtractor cell," Proceedings of the 27th IRF International Conference, Chennai, India, June 2015.
[2] Anindya Ghosh and Debapriyo Ghosh, "Optimization of static power, leakage power and delay of full adder circuit using dual threshold MOSFET based design and T-Spice simulation," IEEE International Conference on Advances in Recent Technologies in Communication and Computing, 2009.
[3] Prateek Mishra, Anish Muttreja, and Niraj K. Jha, "FinFET circuit design," Springer Science Business Media, 2011.
[4] M. Jurczak, N. Collaert, A. Veloso, T. Hoffmann, and S. Biesemans, "Review of FinFET technology," IEEE International Conference on IC Design and Technology, 2009.
[5] M. Vamsi Prasad and K. Naresh Kumar, "Low power FinFET based full adder design," International Journal of Advanced Research in Computer and Communication Engineering, vol. 6, no. 8, Aug. 2017.
[6] Ahmed M. Shams, Tarek K. Darwish, and Magdy A. Bayoumi, "Performance analysis of low power 1-bit CMOS full adder cells," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 10, no. 1, Feb. 2002.
[7] Anish Muttreja, Niket Agarwal, and Niraj K. Jha, "CMOS logic design with independent gate FinFETs," IEEE International Conference, 2007.
[8] Raju Hajare, "Performance enhancement of FinFET and CNTFET at different node technologies," Microsystem Technologies, vol. 21, no. 4, Apr. 2015.
[9] Jerry G. Fossum and Vishal P. Trivedi, Ultra-Thin-Body MOSFETs and FinFETs, Cambridge University Press, 2013.
[10] International Technology Roadmap for Semiconductors (ITRS), "ITRS Reports," Available: http://www.itrs.net
[11] Yingtao Jiang, Abdul Karim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, "A novel multiplexer-based low power full adder," IEEE Transactions on Circuits and Systems, vol. 51, no. 7, July 2004.
[12] Likhitha Dhulipala and Lourts Deepak A., "Design and implementation of 4-bit ALU using FinFETs for nanoscale technology," IEEE Conference, 2011.
[13] Sumeer Goel, "Design of robust, energy-efficient full adder for deep-submicrometer design using hybrid CMOS logic style," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 12, Dec. 2006.
[14] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE Journal of Solid-State Circuits, 1997.
[15] M. M. Islam and M. Hasan, "Design of a low power 8T full adder cell using CNTFET," International Journal of Computer Applications, 2011.
[16] B. D. Liu, C. H. Tsai, and S. Y. Chen, "Low-voltage low-power CMOS full adder cells," IEEE Transactions on Circuits and Systems II, 2004.
[17] Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill.
[18] Yuan Taur and Tak H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press.