IJRAR.ORG E-ISSN: 2348-1269, P-ISSN: 2349-5138

INTERNATIONAL JOURNAL OF RESEARCH AND ANALYTICAL REVIEWS (IJRAR) | IJRAR.ORG

An International Open Access, Peer-reviewed, Refereed Journal

Switched Capacitor Multilevel Inverter for Transformerless Grid-Connection Applications

N. Srilatha

Department of Electrical Engineering,
Osmania University, Hyderabad, India

Abstract : This research introduces a novel configuration for the switched-capacitor multilevel inverter (SCMLI) designed specifically for photovoltaic systems, aiming to mitigate leakage current. In this configuration, capacitors are harnessed as a virtual DC power source to amplify the input voltage. All capacitors are charged uniformly based on the DC source, streamlining the need for just a single DC source to achieve the desired staircase waveform. In this setup, to generate negative voltage levels, the capacitors are connected to the output in reverse polarity. Consequently, the traditional H-bridge circuit used in standard SCMLIs for generating zero and negative voltage levels, along with its associated variable common mode voltage, is eliminated. Through direct linking of the load's ground terminal to the negative polarity of the photovoltaic system, the issue of leakage current is effectively addressed. Furthermore, this topology excels in redirecting reverse currents and producing an output waveform spectrum of acceptable quality. To comprehensively assess the functioning states of all components and calculate losses, the study employs simulation through MATLAB-SIMULINK software.

Index Terms **- Common mode voltage, Leakage current, Multilevel inverter, Switched capacitor.**

I. INTRODUCTION

A significant number of individuals who utilize solar energy tend to feed excess energy back into the electrical grid. Photovoltaic systems that are connected to the load can be categorized into two distinct groups: those with transformers and those without. In systems incorporating transformers, there exists galvanic isolation between the photovoltaic panels and the load. However, this setup results in increased costs, larger sizes, and power losses. Consequently, adopting transformerless systems offers a noteworthy advantage for enhancing the overall efficiency of the setup. Nonetheless, a crucial challenge in transformerless grid-connected systems is the adverse impact stemming from leakage current, which arises due to the presence of parasitic capacitors between the PV panels and the ground.

Multilevel voltage source inverters (MLVSIs) have gained significant popularity as an effective solution for integrating renewable energy sources like wind turbines, photovoltaic cells, and electric vehicles (EVs), as well as for advanced adjustable speed drives and various emerging power electrical applications. This class of converters offers the advantage of reducing voltage stresses on switches and minimizing electromagnetic interference (EMI) by producing a staircase-like voltage waveform with an increased number of voltage levels. Moreover, the resulting staircase waveforms at the output contribute to a reduction in total harmonic distortion (THD). Consequently, in order to achieve an acceptable THD level, these inverters require a smaller-sized output filter, consequently leading to a reduction in inverter dimensions. Switched-capacitor multilevel inverters (SCMLIs) possess the capability to amplify input voltage, and they are capable of generating multilevel staircase waveforms at the output, thus eliminating the necessity for a bulky filter.

The basic structure of a single-phase load-connected inverter and the Common Mode (CM) current path are shown in Fig 1(a), where P and N indicate positive and negative polarity of the PV panel respectively. In this case, ZG and CPV refer to the ground impedance and the parasitic capacitance between the PV array and the ground. This CM voltage and the caused leakage current may lead to safety threats and reduce the efficiency as well as increase the grid current distortion. Fig 1(b) illustrates the facilitated equivalent scheme of the CM resonant current. The CM voltage is given by

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} + (v_{AN} - v_{BN})\frac{L_2 - L_1}{2(L_1 + L_2)} \quad (1)$$

Where v_{AN} and v_{BN} are considered as the voltage difference between terminal A and B, which constitutes the inverter's output, relative to the neutral point of the PV cell. Clearly, maintaining a consistent common mode voltage leads to a decrease in leakage current. To attain this outcome, in the design of full-bridge inverters like " H5 inverter, H6 inverter, HERIC inverter, etc., two inductors having identical values (L1=L2) are used as the output filter. Thus, the equation of common mode voltage will be simplified as follows:

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = Constant \quad (2)$$

Within this approach, the output filtering setup incorporates a pair of inductors utilizing distinct cores, resulting in an augmented size and elevated expenses. An alternative avenue involves adopting half-bridge inverter variants, exemplified by the neutral point clamped (NPC) inverters. This choice serves to uphold a consistent common mode voltage. Consequently, this adjustment eradicates one of the inductors (or reduces it to zero), thereby retaining the employment of a sole inductor as an output filter.

In this case, the relationship of the common mode voltage is defined as:

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} + \frac{v_{AN} - v_{BN}}{2} \quad if: L_1 = 0$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} - \frac{v_{AN} - v_{BN}}{2} \quad if: L_2 = 0 \qquad (3)$$

In contrast to full-bridge configurations, a downside of this design lies in the necessity for dual DC bus voltages. Fig 2 shows topologies of the grid-connected inverter based on full-bridge and half-bridge power converter structures. Conversely, traditional switched-capacitor inverters encounter challenges due to the utilization of the H-Bridge circuit for generating negative polarity voltage levels in the output. This results in a fluctuating common mode voltage, consequently giving rise to leakage current. Therefore, additional circuit components are necessary to achieve a consistent common mode voltage.

Employing a shared ground (CG) represents an efficient approach for eradicating leakage current. To achieve this objective, the negative terminal of the PV panel is directly linked to the grid's neutral line. This arrangement guarantees the stabilization of the common mode voltage, effectively eliminating any instances of leakage current. In recent years some modified switched-capacitor inverters have used this solution to cancel the leakage current. Generally, In the context of three-level inverters, when the capacitor is not connected in parallel with the voltage source across two consecutive levels, there is a substantial augmentation in the voltage fluctuations of the capacitor.

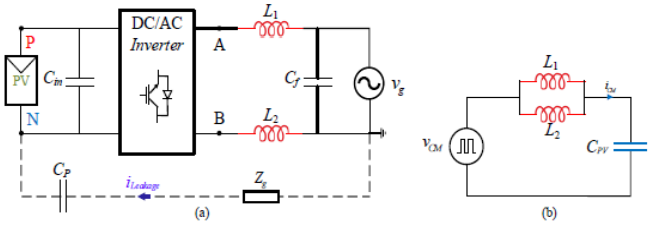

Figure 1. Basic structure of the single-phase grid-tied inverter: (a) CM current path, (b) equivalent scheme

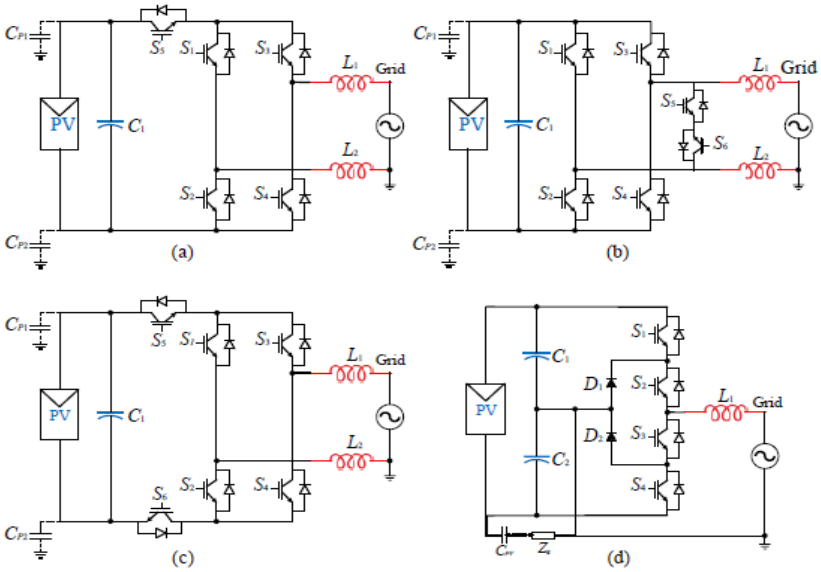

Figure 2. Full-bridge and Half-bridge topologies for grid-connected transformerless inverters:
(a) H5 inverter (b) HERIC inverter (c) H6 inverter with DC bypass (d) NPC half-bridge inverter

Fig 3(a) illustrates an inverter structure, which uses this technique and include of five power switches. In this topology, the capacitor at zero and +VDC levels goes in parallel with the source. Meanwhile, due to the circuit structure and the use of conventional switches, which also can flow the reverse current, it has the capability to be utilized as a reactive load. The flying capacitor transformerless inverter as shown in Fig 3 (b) has reduced the number of controllable elements of the topology. In this structure, there are two paths to charge the capacitor, while it makes +VDC and negative zero levels in output. However, for the inductive load, the current of the inductor cannot change quickly. Thus, the capacitor is in the path across the load and the current passes within the capacitor whilst the output is switching to positive zero level and then increases its voltage. Therefore, in re-switching to +VDC level, the capacitor cannot be tuned by DC source. In addition, at the negative level, as long as there is the reverse current, it will path through the capacitor (depending on the power factor), thus, the voltage variation of the capacitor raises. Fig 3 (c) shows the charge-pump topology which is proposed to resolve the abovementioned problem. In this design, the capacitor that produces the negative output voltage level sets to the input source at the zero level, and the issue of increased voltage variation, is eliminated. Meanwhile, another path is considered for the reverse current. Thus, the reverse current does not pass through the capacitor. Siwakoti-H inverter topology, which is shown in Fig 3 (d), only consists of four switches and uses the lowest power semiconductor devices in comparison with other presented topologies. However, in the reactive power, there are the same problems as the flying capacitor inverter introduced in Fig 3 (b). At the positive cycle, the capacitor cannot regulate by the DC source. Moreover, at the negative cycle, it has reverse current. Thus, the circuit suffers from the increasing of capacitor voltage variation. Moreover, all the inverter structures mentioned above are only able to produce three-level output waveform. Therefore, boost circuit has to be added.

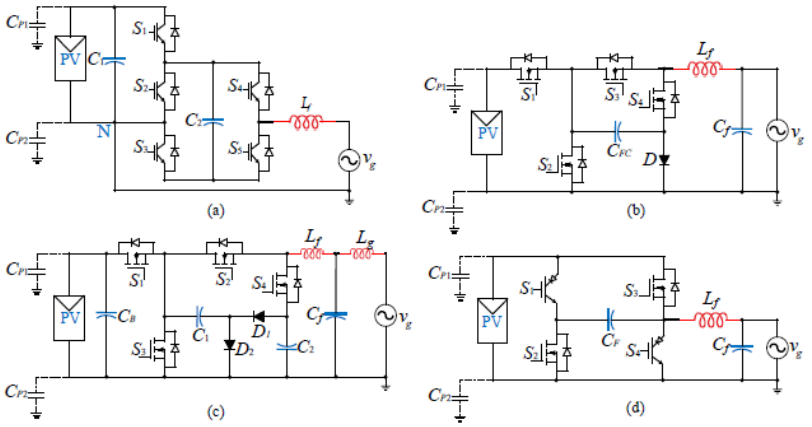

Figure 3. Common-Ground (CG) topologies for grid-connected inverters:
(a) CG inverter (b) Flying Capacitor CG Inverter (c) Charge Pump CG Inverter (d) Siwakoti-H inverter

By considering the above-mentioned problems, this paper presents a novel switched-capacitor multilevel inverter topology, which has the potential to boost voltage as well as to eliminate the leakage current. The basic unit of the topology contains four power switches and one capacitor.

This novel circuit design offers several distinct advantages. Firstly, it operates efficiently with just a single input voltage source, thereby negating the necessity for a boost circuit that would otherwise contribute to increased size and costs. Secondly, the symmetric structure within the topology enables each additional capacitor to be charged in alignment with the input voltage, facilitating the attainment of two voltage levels at the output and thereby augmenting the maximum output voltage achievable.

Furthermore, conventional switched-capacitor multilevel inverters (SCMLIs) rely on an H-bridge circuit to generate negative output levels, which inadvertently introduces a variable common mode voltage, consequently resulting in leakage current. In stark contrast, the proposed SCMLI directly establishes a connection between the grid's neutral point and the negative polarity of PV panels, leading to the establishment of a common ground within the circuit. This innovative approach ensures the complete elimination of leakage current.

Lastly, this comprehensive study introduces refined equations characterized by a high degree of accuracy. These equations serve as powerful tools for the precise computation of switching losses, conduction losses, and losses stemming from the voltage drop across the capacitors' equivalent series resistance (ESR). This methodological enhancement significantly enhances the precision and predictive capacity of loss calculations in the considered system.

II. Proposed Topology

The topology in Figure 4 illustrates the basic circuit of the SCML inverter. It should be noted that Sa includes two groups of unidirectional switches. The capacitors C1 and C2 are charging equally the DC source when the group of the switches Sa, S1 and S2 become ON and the other switches are OFF. In this state, the positive and negative polarity of C1 and C2 are connected to each other respectively, and two capacitors are in parallel.

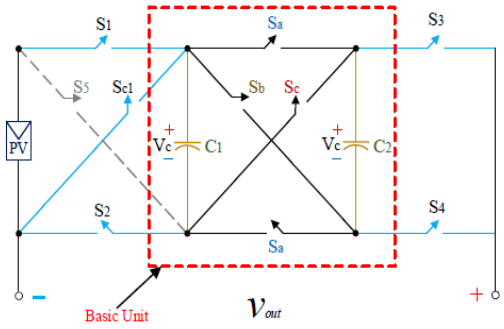

Figure 4. Basic topology for the SCMLI

Another Condition happens when Sb becomes ON, and other switches are OFF. Here, the positive polarity of C1 is connected to the negative polarity of C2. In this situation, if S3 and S2 become ON, the capacitors C1 and C2 will be in series to the load and generate a higher positive level in the output. In the last state, if Sc along with S2 becomes ON (other switches of the unit were OFF), the negative polarity of C1 is connected to the positive polarity of C2 and if S4 was ON, thus, the stored voltage in the capacitor C2 is pumped to the output in reverse polarity. In fact, during the generation of positive and negative output voltage levels, S3 and S4 become ON respectively. In this structure, the DC power supply does not have a direct role to generate negative output levels. However, if the switch S5 becomes ON, the DC source will be series with the capacitor; thus, it can make an extra positive output level rather to the negative levels. This state disturbs the symmetrical output waveforms. Thus, the switch S5 is eliminated in order to prevent this state.

III. Design of 9-Level SCMLI

According to the generalized structure, the topology of the 5-level inverter, which comprises of one input voltage source, two capacitors, nine switches (seven ordinary switches and two unidirectional switches), is shown in Figure 6(a). In this case, unidirectional switches are utilized to charge the capacitors, which are located in higher stages, and when these kinds of switches are ON, the switches of Sb and Sc group will be OFF. On the other hand, it is noteworthy that the switches of Sa group make the capacitors charging path. The switches of Sb group make a series the capacitors with positive polarity. Moreover, while the Sc category switches are turning ON, the capacitors will be series with negative polarity to generate the negative levels. To confirm the functionality of proposed circuit in generating more output voltage levels and comparing with the similar structures in terms of the number of output levels, the 9-level structure of the inverter based on the topology is introduced and analyzed, as shown in Figure 6(b). On the other hand, the states of the switches and capacitors in the 5-level is similar to the state of the switches in the 9-level circuit to make the same output levels, so the analysis of the 9-level inverter also includes the function of the switches in the 5-level inverter.

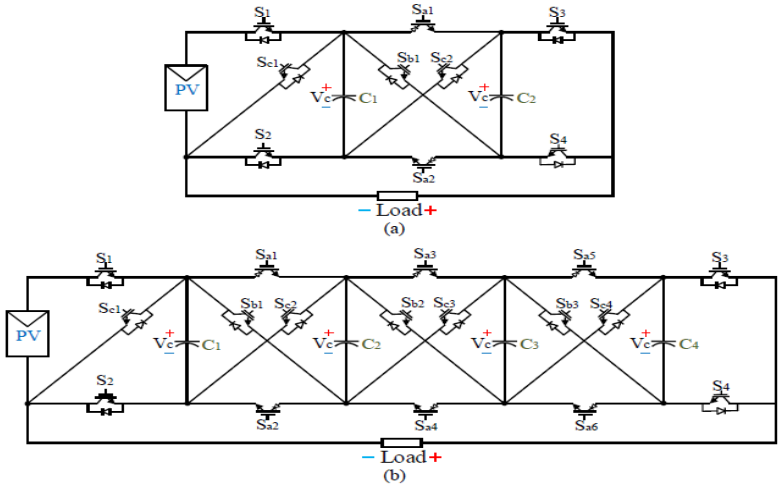

Figure 6. DC-AC inverter. (a) 5-level inverter, (b) 9-level inverter

IV. Control Structure

In the switched-capacitor inverter in order to form the zero level, all Sa group switches (unidirectional switches) are ON, and all capacitors are charging as much as the input voltage source. In this case, the switches S3 and S4 are OFF and ON respectively. Regarding the use of unidirectional switches in the circuit, there are two paths for forward and reverse current in the loop. The direction of the reverse flow caused by the inductive load marked in blue and the path of the working states of the inverter to determine the output voltage levels, as well as the charging path of the capacitors, are specified in red line. In addition, from this figure the different status of the capacitors in terms of charging/discharging are apparent. As it can be seen, the switches of the Sc group connect the capacitor to the output in reverse polarity to generate the negative output levels, and thus the need of H-bridge is eliminated.

When the +VDC level is forming, all Sa switches are still ON and only the switches S3 and S4 varies mode, and the voltage source directly generates the +VDC level. In this situation, all capacitors are in charging mode same as the zero-voltage level. To make the +2VDC level, Sa5 and Sa6 are switched OFF and switch Sb3 turned ON to pump the capacitor C4 in series with the voltage supply to the output load. Here, the capacitor C4 is in the discharge mode, and other capacitors (C1, C2 and C3) are charged by the DC power supply simultaneously. In the same way, other voltage levels will be created. To form each positive level, the capacitor of the related unit by the switch Sb is connected in series with the voltage source to the output load and the other switches of the unit turn OFF. It should be noted that the capacitor C1 in all states of the production of positive levels is in parallel to the voltage source and is charging, thus it has no role in the creation of positive levels.

In the production of negative output levels, the switch Sc of each unit has illuminated to connect the capacitor of the unit with reverse polarity to the output. To build the first negative voltage level, the stored voltage of the capacitor C4 is pumped through the switch Sc1. In this case, the other capacitors are in charging mode simultaneously. The capacitors C3 and C4 via the switches Sc3, Sc4 and S4 are series connected to the output to generate -2VDC level. In this term, the switches Sa2 and S2 are ON. Continuing this process makes -3VDC level. To create -4VDC level, all switches in the Sc group (Sc1, Sc2, Sc3 and Sc4) with S4 become ON and other switches are OFF. In this state, all capacitors are in discharging mode.

In the proposed SCMLI, the capacitor will be parallel with the source during a time interval and charged equal to the input voltage while the group switches are ON. Then, to build up higher output levels, the stored energy in the capacitor is pumped to the output in series, which leads to decrease the voltage of the capacitor. On the other hand, due to the series connection of the capacitor with the output load at the discharging time, a voltage drop on the capacitor is created which leads to generating the power losses. Here, the charging and discharging of the capacitor by the switching frequency leads to making small, but large quantities of voltage drop.

In the intervals, where the capacitor is continuously connected to the output in series, this causes large voltage drop and effective power losses in comparison with the small voltage drop. According to Fig 7, during two consecutive level ±n and ±(n+1), when the capacitor is in discharging mode; thus, it has an effective voltage drop. This voltage drop leads to generating power dissipation. On the other hand, when the capacitor is discharging continuously (at least in two levels that are sequential), the large voltage drop will have happened. While the capacitor is in charge/discharge mode by switching frequency, the caused voltage drop by this condition is low.

	Reference	ON State Switches	Capacitor state				V_{out}
			C_1	C_2	C_3	C_4	
Positive ref	$ref > e_4$	$S_{b1}, S_{b2}, S_{b3}, S_1, S_2, S_3$	C	D	D	D	$4V_{DC}$
	$e_4 \geq ref > e_3$	$S_{a1}, S_{a2}, S_{b2}, S_{b3}, S_1, S_2, S_3$	C	C	D	D	$3V_{DC}$
	$e_3 \geq ref > e_2$	$S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{b3}, S_1, S_2, S_3$	C	C	C	D	$2V_{DC}$
	$e_2 \geq ref > e_1$	$S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{a5}, S_{a6}, S_1, S_2, S_3$	C	C	C	C	V_{DC}
	$\|ref\| \leq e_1$	$S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{a5}, S_{a6}, S_1, S_2, S_4$	C	C	C	C	0
Negative ref	$e_2 \geq \|ref\| > e_1$	$S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{c4}, S_1, S_2, S_4$	C	C	C	D	$-V_{DC}$
	$e_3 \geq \|ref\| > e_2$	$S_{a1}, S_{a2}, S_{c3}, S_{c4}, S_1, S_2, S_4$	C	C	D	D	$-2V_{DC}$
	$e_4 \geq \|ref\| > e_3$	$S_{c2}, S_{c3}, S_{c4}, S_1, S_2, S_4$	C	D	D	D	$-3V_{DC}$
	$\|ref\| > e_4$	$S_{c1}, S_{c2}, S_{c3}, S_{c4}, S_4$	D	D	D	D	$-4V_{DC}$

* *C*: Charging Mode * *D*: Discharging Mode

Figure 7. States of switches and capacitors in 9-level SCMLI

One of the critical parameters in the design and analysis of power electronics circuits is the calculation of power dissipation. The accuracy of the estimate of this characteristic of the circuit in the technical evaluation and the application of the circuit and thus the final cost has a significant impact. The power losses in the proposed circuit consists of three categories. Power losses due to capacitor voltage drop, switching losses and conduction losses.

IV. RESULTS AND DISCUSSION

This section presents simulation results for the proposed 9-level SCMLI using MATLAB/SIMULINK software. All semiconductor devices are assumed with internal resistance Ron=0.001 Ω. The switches are driven based on the proposed modulation strategy with a switching frequency f_{SW} = 20 kHz and the modulation index M=0.85.

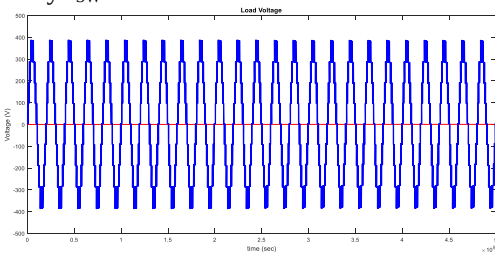

Figure 8 Output voltage of SCMLI for two different loads

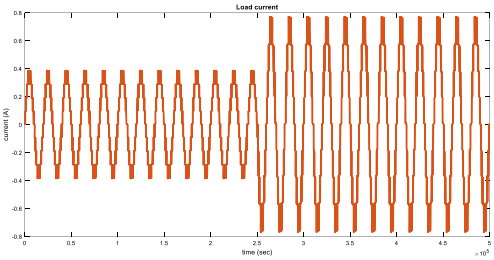

Figure 9 Output current of SCMLI for two different loads

The output volage at the load is maintained constant though there is a change in load as is clearly indicated in Fig 8 and Fig 9.

Table 1 Comparison between H bridge 9-level and SCMLI 9-level w.r.t loads

Parameter	**H-Bridge Inverter**	**SCMLI Inverter**
Number of capacitors	4	4
Number of sources	4	1
Number of switches	16	17
Parasitic capacitance	Present	Not present
Common Mode Voltage	Present	Not present
Leakage Current	Present	Eliminated

Table 2 Comparison between H bridge 9-level and SCMLI 9-level w.r.t parameters

Parameter	**9 Level H bridge Inverter**		**9 Level SCMLI**	
Load	RL	RL	RL	RL
Fundamental Load Voltage (V)(peak)	353	353	344.2	344.2
Fundamental Load current(A)(peak)	0.7	0.612	0.6793	0.5992
THD(%)	7.27	7.27	1.14	1.14

In the above table, comparison is done between H bridge 9 level and SCML Inverters for the values of R=1k ohms &L=0.2H

This study introduces a novel configuration for the switched-capacitor multilevel inverter (SCMLI) that effectively eliminates the occurrence of leakage current. Unlike conventional SCMLIs that rely on an H-bridge circuit to create zero and negative levels, which is hindered by the instability of a variable common mode voltage, the proposed approach eliminates the need for the H-bridge circuit. In this context, the generation of negative levels involves the capacitor releasing its stored energy into the output with reversed polarity. Notably, the direct connection between the neutral point of the grid and the negative terminal of the PV panels establishes a common ground within the circuit, effectively eliminating leakage current. Incorporated within the suggested topology is a sinusoidal pulse-width modulation method that autonomously equalizes the voltage across all capacitors in relation to the DC source. A thorough analysis has been conducted on a nine-level SCMLI. A comprehensive evaluation comparing this new topology to existing circuits demonstrates its exceptional performance in both voltage enhancement and the eradication of leakage current issues.

REFERENCES

[1] N. Vázquez, M. Rosas, C. Hernández, E. Vázquez, and F. Perez-Pinal, "A new common-mode transformerless photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6381–6391, Apr. 2015.

[2] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793–805, Feb. 2013.

[3] Y. Siwakoti and F. Blaabjerg "Common-ground-type transformerless in- verters for single-phase solar photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2100–2111, Mar. 2018.

[4] J. F. Ardashir, M. Sabahi, S. H. Hosseini, F. Blaabjerg, E. Babaei, and G. B. Gharehpetian, "A single-phase transformerless inverter with charge pump circuit concept for grid-tied PV applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5403–5415, Jul. 2017.

[5] L. C. Breazeale and R. Ayyanar, "A photovoltaic array transformer-less inverter with film capacitors and silicon carbide transistors," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1297–1305, Mar. 2015.

[6] A. Kumar and P. Sensarma, "A 4-switch single-stage single-phase buck-boost inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5282–5292, Jul. 2017.

[7] R. Barzegarkhoo, S. S. Lee, Y. P. Siwakoti, S. A. Khan, and F. Blaabjerg, "Design, control, and analysis of a novel grid-interfaced switched-boost dual T-type five-level inverter with common-ground concept," *IEEE Trans. Ind. Electron*, to be published, doi: 10.1109/TIE.2020.3018073.

[8] N. Vosoughi, S. H. Hosseini, and M. Sabahi, "A new single phase transformerless grid connected inverter with boosting ability and com- mon ground feature," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9313–9325, Nov. 2019.

[9] N. Vosoughi, S. H. Hosseini, and M. Sabahi, "Single-phase common- grounded transformerless grid-tied inverter for PV application," *IET Power Electron.*, vol. 13, no. 1, pp. 157–167, Jan. 2020.

[10] F. B. Grigoletto, "Five-level transformerless inverter for single-phase solar photovoltaic applications," *IEEE Emerg. Sel. Top. Power Electron* ., vol. 8, no. 4, pp. 3411–3422, Dec. 2020.

[11] F. B. Grigoletto, "Multilevel common-ground transformerless inverter for photovoltaic applications," *IEEE Emerg. Sel. Top. Power Electron*., vol. 9, no. 1, pp. 831–842, Feb. 2021.

[12] Barzegarkhoo, Y. P. Siwakoti, and F. Blaabjerg, "A new switched- capacitor five-level inverter suitable for transformerless grid-connected applications," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8140–8153, Aug. 2020

[13] R. Barzegarkhoo, Y. P. Siwakoti, N. Vosoughi, and F. Blaabjerg, "Six- switch step-up common-grounded five-level inverter with switched- capacitor cell for transformerless grid-tied PV applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1374–1387, Feb. 2021.

[14] K. Takahashi, and H. Koizumi, "A common ground five-level inverter using switched capacitor," in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc.*, 2019, pp. 1485–1489.

[15] N. Vosoughi, S. H. Hosseini, and M. Sabahi, "A new transformer-less five-level grid-tied inverter for photovoltaic applications," *IEEE Trans. Energy Convers.*, vol. 35, no. 1, pp. 106–118, Mar. 2020 [21] H. Xiao and S. Xie, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1799–1808, Apr. 2012.

[16] V. Sonti, S. Jain and S. Bhattacharya, "Analysis of the Modulation Strategy for the Minimization of the Leakage Current in the PV Grid-Connected Cascaded Multilevel Inverter," IEEE Trans. Power Electron., vol. 32, no. 2, pp. 1156–1169, Feb. 2017.

[17] C. Woo-Jun, "Evaluation and analysis of transformerless photovoltaic inverter topology for efficiency improvement and reduction of leakage current," IET Power Electron., vol. 8, no.2, pp. 255–267, 2015.

[18] Y. P. Siwakoti; F. Blaabjerg, "A novel flying capacitor transformerless inverter for single-phase grid connected solar photovoltaic system" IEEE 2016 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pp. 1-6, 2016.