DESIGN AND IMPLEMENTATION OF 2-BIT COMPARATOR USING QCA

T. Paidi Raju¹, I. Hemanth Kumar², K. Lokesh Krishna³, P. Ravi Kumar⁴, M. Saritha Devi⁵
Dept. of Electronics & Communication Engg.¹, ², ³, ⁴, ⁵
UG Scholar², ³, ⁴, Assistant Professor⁵
Godavari Institute of Engineering and Technology, Rajahmundry, AP, India¹, ², ³, ⁴, ⁵

Abstract: Quantum-dot cellular automata (QCA) are one of the most promising emerging Nano electronic paradigms used for designing computers and very large-scale integration circuits. Comparator is a hardware electronic device and made up of standard AND, OR and NOT gates. This device takes n number of inputs in binary form and determines whether one input is greater than, less than or equal to other input. CMOS Comparators has a major drawback of size and power consumption leading to the failure of Moore’s law. To overcome this disadvantage, Quantum-Dot Cellular Automata, an emerging Nanotechnology has been implemented. QCA provides faster speed with low power dissipation at nano-scale extent. In this paper mainly design of QCA-based 2-bit comparator with less latency in lesser area. Finally, in this paper developed the existing and proposed comparator layout and simulation by using QCAD software.

Index Terms – QCA Technique, Comparator, Quantum computing.

I. INTRODUCTION

A cellular automaton (CA) is a discrete dynamical system consisting of a uniform (finite or infinite) grid of cells. Each cell can be in only one of a finite number of states at a discrete time. As time moves forward, the state of each cell in the grid is determined by a transformation rule that factors in its previous state and the states of the immediately adjacent cells (the cell’s “neighborhood”). The most well-known example of a cellular automaton is John Horton Conway's "Game of Life", which he described in 1970 in recent years, the complementary metal-oxide- semiconductor (CMOS) technology has been shown to have high power consumption and current leakage. Further more, it has been associated with numerous problems in making CMOS circuits smaller; such examples are various physical phenomena, the specific mass of each element, and quantum effects that disrupt the normal function of transistors. With this background in mind, researchers have been attempting to develop small-scale technologies with low power consumption and current leakage. Quantum-dot cellular automata (QCA) are an emerging nano electronic technology, which have recently been reported to have a more efficient performance. Although designing QCA circuits is far more challenging than the CMOS technology, there has been growing interest in the simple structure of these circuits, as well as the variety of the methods used for their design and manufacturing. Design of the novel approximate XOR gates has been presented. It also describes the simulation parameters used to verify the design of the proposed 2-bit comparator and the evaluation of the results.

Any device designed to represent data and perform computation, regardless of the physics principles it exploits and materials used to build it, must have two fundamental properties: distinguish ability and conditional change of state, the latter implying the former. This means that such a device must have barriers that make it possible to distinguish between states, and that it must have the ability to control these barriers to perform conditional change of state. For example, in a digital electronic system, transistors play the role of such controllable energy barriers, making it extremely practical to perform computing with them.

The major objective of this work is to evaluate and explore the 2-bit comparator with the modified approach with a focused goal on 2-bit existing comparator performance in addition to less delay, spatial area reduction. The designing of existing and proposed 2-bit comparator and results is noted by utilizing the Q-CAD tool. Predominantly less delay in addition to the reduce the number of quantum cells is the main intention of this work. Furthermore, the design is made in such a way it must reliable as well as should have less in complexity. Since a less number of quantum cells are put into operation in the small area and the delay is reduced. The modified architecture of 2-bit comparator circuit is designed using Q-CAD tool and corresponding layout are obtained.

This paper contribute five sections, in first section give the brief introduction of QCA Technique see above section, Literature Survey and Existing Comparator explanation see in section two and three, section four and five give the Proposed comparator and results discussion and finally see the conclusion in section six.

II. LITERATURE SURVEY

In general, comparator finds application in most of the Digital Communication systems, processors, sorting of data and Analog to Digital conversion, Image processing, etc. Initially, a Serial-Bit Stream Analyzer (SBSA) using QCA was proposed by Janulis JR et al., (2004). The SBSA design, which was shown, requires a shift register and a multiple-bit comparator [1]. It is used to identify any random bit pattern appearing on its serial input. The SBSA compares the serial data with the available bit pattern, which was already at the other input of the comparator. The SBSA design generates output as ‘1’ if two-bit patterns are equal; otherwise, it produces output as ‘0’. The SBSA is used in telecommunications for detection of header packets on transmitted data. This design simply uses XOR operation as a comparator along with the 1-bit shift register as a bit slice. The authors suggested that the SBSA design could be extended to compare any number of inputs by replicating the bit slices. Whereas, the SBSA design occupies more area with higher clock zones. The configurations suggested [2-10] offer higher computational efficiencies, and circuits are capable of distinguishing all the three probable conditions. The three states are named as equality, lesser than, and greater than (here so-called full comparators) are demonstrated [2], [3], and [6]. The 1-bit comparator implementation has presented by Qiu K and Xia Y (2007). This 1-bit comparator was implemented by using XOR gate and NOT gate [2]. The authors, Xia Y and Qiu K (2008) refined the 1-bit comparator design by using the universal logic gate (ULG) [3]. This strategy does not detect the equality case thus it cannot be categorized as a full-comparator. Lampreht B et al., (2008) have designed a serial comparator. Whereas, this design performs the full comparator functionality with more delay [4]. Wagh MD et al., (2008) has exploited a tree-based architecture.

However, the proposal of n-bit comparator strategy can identify only A>B or A = B where A and B are n-bit inputs [5]. Xia Y and Qiu K (2009) have upgraded the 1-bit comparator design in [2] to design an n-bit parallel comparator [6]. The modular ULG2 design
based full comparator was presented by Ying SY et al., (2010) [7]. The authors design a ULG.2 gate to reduce the wire crossings. Hence, this design reduces the number of cells compared to the earlier design [2]. Hayati M and Rezaei (2012) have presented an optimized full comparator [8]. This design shows a significant improvement of cell count, area, and delay over the other existing designs. Whereas the optimized 1-bit full comparator design uses additional input, the output OA=B of one stage is fed directly to this input of the next stage to implement the n-bit full comparator. Ghosh B et al., (2012) designed a QCA magnitude 1-bit comparator with the conventional basic logic functions and 2-cell inverter structure [9]. Further, by using this 1-bit comparator, 2-bit and 3-bit comparators were projected by taking the parallel data inputs. All the outputs of 1-bit comparators are applied to additional ANDOR logic to generate the final outputs of 2-bit and 3-bit comparators. Perri S et al., (2014) designed the efficient binary comparators in QCA. The authors proposed two architectures named as Cascade-Based (CB) and Tree based (TB) architecture [10]. The two designs are implemented by the exploitation of four theorems and two corollaries to increase the performance of full comparators. The theorems were extended to design the n-bit full comparators. To design n-bit comparators, the operands 1− an=A(n−1:0) ...0 and B(n−1:0) 1− b= ...b0 are divided into a suitable number of 2-bit and 3-bit subwords and theorems 1 and 2 are applied to relate these subwords. Further, theorems 3 and 4 composed with Corollaries 1 and 2 are employed to process the intermediate outcomes attained the subwords. Among the other existing comparator architectures the strategies presented by Perri S et al., requires less area and cell count with higher speed and well suited for parallel full comparators [10]. The high-speed binary comparator proposed by Mathiazhagan R et al., (2014) uses a decision block and CLA adder method [11]. In this approach, the input bits were fragmented into groups and equality checking begins with Most Significant Bit (MSB) group by using XOR operation, if the MSB group is equivalent, the checking continues to the following consecutive set of Least Significant Bit (LSB) group. If two groups were not equal, the encoder part finds the greater number of the given two numbers by utilizing the carry out of CLA. However, this method has been realized with the aid of Verilog code and verified by using XILINX ISE 9.2. Thus, this approach was not able to give the performance parameters of the design in QCA technology regarding cell count, area, and delay to compare this design with the other existing designs. By observing the various existing comparator designs [1-11], A. Mallaiha, G. N. Swamy, K.Padmapriya (2017) [12] proposed a high speed comparator with clocking method 180 out of phase clock crossover to outline the 1-bit comparator and compare with the current outcomes. The new proposed wire crossing plan lessens the quantity of cells required to configuration, power and area necessities. Additionally, we planned 2-bit comparator having 11 majority gates (voters), 2 number of crossovers with 0.38 μm² area, 203 number of cells. The designed 1-bit comparator contrast and the past outcomes where cells, region, delay demonstrates 53.57 %, 50 % and 33.32 % improvement respectively, most of the works are focused on the 1-bit comparators and parallel comparators. Whereas, it is noticed that the attention paid towards the serial bit stream data comparison is limited. Moreover, the existing methods in serial bit stream comparison [1, 4] suffer from the limitation of speed. Thus, the proposed work is motivated to design a high speed and area efficient 2-bit comparator.

III. EXISTING COMPARATOR

QCA Designer is a layout and simulation tool for Quantum-Dot Cellular Automata developed at the ATIPS laboratory at the University of Calgary. Many of QCA Designer features can be intuitively discovered without the aid of a manual. This manual will be brief and to the point. Although still a relatively new area of research, nanotechnology has attracted many of the top researchers around the world. Much of the new interest in nanotechnology is a result of the significant increase in capability of fabrication. The leading semiconductor industry analysis groups such as the International Roadmap for Semiconductors (ITRS) report a significant acceleration in the increase of fabrication capability. The ITRS has changed its prediction of the physical gate length of MOS transistors by 2005 from 60nm in 1999 to 32nm in 2000. Many researchers see this as an opportunity to begin research in nanotechnology that they may not have considered earlier. As a result, many new technologies for computing have emerged recently. As well, many researchers predict the possibility of a significant slowdown in the advancement of MOS technology at Nano-scales. At such scale quantum phenomena can no longer be simply averaged out and quantum effects begin to take control of transistor function. Many nanotechnology researchers feel that these problems will not result in a slowdown of advancement in electronics but rather in an opportunity for novel technologies. To date, CMOS circuits have a monopoly on the microelectronics industry, and most are quite comfortable with this well-established technology. Some of the technologies with most potential are Quantum-dot cellular automata (QCA), resonant tunneling diodes, and carbon Nano-tubes. One of the two fundamental building blocks of each QCA circuit is the inverter. Fig. 1 (on the left) shows the basic QCA inverter gate. In this gate, the signal enters from the left and divides into two QCA wires, which will merge eventually. Complement of the entered signal is calculated at the merge time and released to the right. In fact, as a result of the Coulomb force, the stable state of the output in this structure is the complement of the input.

Fig. 1 layout design of not gate

Another fundamental building block of a QCA circuit is the majority gate. Due to the programming capability of this block, the gate can be used to design various structures. The three-input majority gate consists of three inputs, an output, and a work cell. The work cell will be polarized based on the majority polarizations of the cells, as well as the repulsive force among the three input cells.

Logical function of this gate is presented as follows.

\[ M(A, B, C) = AB + AC + BC \]

According to the logical function of the majority gate, if the constant value of –1 (representing logical zero) is assigned to the input cell C, it will function as the two-input AND gate M (A, B, 0) = AB + (A) (0) + (B) (0) = AB Additionally, if the constant value of +1 (representing logical one) is assigned to the input C, it will function as the two input OR gate M (A, B, 1) = AB + (A) (1) + (B) (1) = A + B Each QCA circuit is controlled by the clock mechanism. Synchronization of the majority gate is achieved when all the input signals are applied to the circuit at the same clock zone and related diagrams is shown in Fig. 2.
The timing of QCA, follow the semi adiabatic timing system. This system consists of four stages: switch, hold, release (discharge) and relax (unwind). At first, when the potential energy of the electron is low and the electron isn’t equipped for burrowing between quantum dots, it has a definite extremity. With the start of the switch stage, the potential vitality of electrons begins to rise and toward the finish of this stage the electron achieves its most extreme potential vitality. Amid the hold stage the electron keeps up its greatest potential energy and turns out to be totally delocalized losing its polarity. In the discharge stage the potential energy of the electron begins to decrease and the cell moves incrementally towards a definite polarity. Amid the last stage i.e. the unwind stage the electron keeps up least energy and is excessively powerless, making it impossible to burrow between the dots. Along these lines, the cell achieves a definite extremity. Each QCA engineering involves four clock zones, if not less, each of which contains the above said four clock stages. Each check zone is out of stage with the following check zone as appeared in Fig. 3(a). The different check zones in a QCA design are spoken to by different hues. The shading codes we have utilized is appeared in Fig. 3(b) [12].

Here we demonstrated the new format engineering of EX-OR entryway consisting of 13 cells with 1/2 clock delay (Fig. 4). This composed EX-OR gate extremely helpful to limit the QCA facilitate format regarding number of cell and clock delay.

The essential function of a comparator is to regard the magnitude of two binary data to determine their relationship. The EX-NOR gate can be utilized as a fundamental comparator in light of the fact that its output is a 1. On the off chance that the two information bits are equivalent and a 0 if the information bits are not equivalent. The logic equations for a 2 bit comparator outputs is as follows:
The logic equations for an existing 2 bit comparator outputs is as follows [12]:

\[
\text{Output}(A < B) = \overline{A_0.B_0}.A_1 \oplus B_1 + A_1.B_1 \\
\text{Output}(A > B) = A_0.\overline{B_0}.A_1 \oplus B_1 + A_1.B_1 \\
\text{Output}(A = B) = A_1 \oplus B_1. \overline{A_0} \oplus B_0
\]

Existing 2-bit comparator logic diagram using majority gates is shown in Fig. 5. Existing 2-bit comparator consists of two EXOR type majority gates and 9 exact majority gates and four inverters. The operation of existing comparator is same as conventional 2-bit comparator but only difference is instead of logic gates, we can use majority gates. Existing comparator gives the better area, power and delay compared to conventional comparator design using CMOS Transistors.

IV. PROPOSED COMPARATOR

The logic equations for an existing 2 bit comparator outputs is as follows:

\[
\text{Output}(A < B) = \overline{\text{XMV}}(\text{XMV}(A_1,B_1,-1),\text{XMV}(A_1,B_1,-1),1) \\
\text{Output}(A > B) = \text{MV}(\text{XMV}(A_0,B_0,-1),\text{XMV}(A_1,B_1,-1),1) \\
\text{Output}(A = B) = \text{MV}(\text{XMV}(A_1,B_1,-1),\text{XMV}(A_0,B_0,-1),-1)
\]

Here, \( \text{MV} \) represents the three input majority gate, \(-1\) represents logical “AND” operation and \( \text{XMV} \) is the three input exclusive-OR gate.
Proposed 2-bit comparator logic diagram using majority gates is shown in Fig. 6. Proposed 2-bit comparator consists of three EXOR type majority gates and 5 exact majority gates and 5 inverters. The operation of proposed comparator is same as conventional 2-bit comparator but only difference is instead of logic gates, we can use majority gates. Proposed comparator gives the better area, power and delay compared to Existing Comparator.

V. RESULTS AND DISCUSSION

we demonstrated Existing and Proposed 2 bit comparator composed utilizing QCADesign programming with wire crossing uses an inverse clock (180 phase shift) system and actualized with most recent EX-OR entryway used in Existing Comparator. The proposed comparator designed by recent EXOR gates thus way reduces the area and delay. Layout of Existing comparator is shown in Fig. 7 and proposed comparator layout and simulation output is shown in Fig. 8 and Fig. 9. Comparison of Existing and proposed comparator is shown in Table 1.

Fig. 7 Layout diagram of Existing Comparator

Fig. 8 Layout diagram of Proposed Comparator
VI. CONCLUSION
The more significant part of QCA combinational circuits with coplanar or multilayer wire crossing it have many-sided outline quality is more. In this project we proposed a smaller 2-bit comparator with no crossing the wires. We composed this QCA design in the QCAD Designer test system. The proposed 2-bit comparator layout cell count less than 44.33 % of most recent outline and area occupation are less than 63.15 % with delay utilizes just 13/4 clock compare to existing 2-bit comparator. Generally, QCA circuits have incredibly noteworthy wiring delays for a quick plan in QCA, many-sided quality imperatives are exceptionally basic issues and the outline needs to utilize compositional systems to support the speed considering these limitations. The QCA innovations once realized will probably require a change in the outline rules. These outlines utilized the given particular plan rules, however as in a CMOS plan they can be scaled in a similar manner. This provides a chance to contrast the abnormal state outline engineering and in QCA circuits.

References