DESIGN OF ASYMMETRIC 15 LEVEL MULTI LEVEL INVERTER USING PD, POD, APOD PWM TECHNIQUES

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Abstract: In recent trends, the electrical power industry is showing tremendous growth and interest in the field of Multi Level Inverters (MLI). With the help of MLI it is easy to produce high power, high output voltage with less number of switching devices and fewer harmonics which is applicable for most of the applications. In this paper, a new inverter topology is proposed which generates fifteen levels of output voltage with using only seven numbers of switches. In order to get fifteen levels of output voltage, various PWM Techniques like alternate phase opposition disposition(APOD), phase disposition(PD), phase opposition disposition(POD) were adopted and THD analysis of those techniques are presented in this paper using MATLAB / SIMULINK software.

Index Terms **–Asymmetric Multi Level Inverter, THD, Logic gates, PD, POD, APOD.**

I. INTRODUCTION

In the present day scenario, as there is a wide range in the usage of renewable energy sources, power electronic converters are in high extent of usage. These power electronic converters especially Multi Level Inverters helps in the integration of renewable energy source and the grid. There is an increase in wide range of families of inverters [1] such as Diode clamped, Flying Capacitor, and Cascaded H Bridge which are associated with single DC voltage source for neutralization. Multiple numbers of DC sources are associated with modular cascaded H Bridge MLI, Hybrid MLI configurations. The necessity of using these different configurations of MLI is that they are capable of giving high output power with the medium voltage sources.

Many research works [2],[3] showed that the design of MLI gives high output voltages with the advantage of providing minimization in switching losses, lower harmonics which paved a way for the implementation of new configurations of MLI with reduced number of switches. MLI can be symmetric or Asymmetric types based on the ratio of DC voltage sources used in the design. If the DC voltage sources are same then it is represented as symmetric topology whereas usage of different dc voltage sources depicts asymmetrical topology of inverters. Design of asymmetrical multi level inverters produces high value of output voltage than symmetrical type of configuration if same number of switches is considered. This became an interesting reason and increased focus on asymmetrical type of configurations.

Various modulation techniques [4], [5] are adopted such as Sinusoidal Pulse with modulation, Advanced Phase Width Modulation, phase shifted modulation in order to operate symmetric and asymmetric MLI with reduced number of switches. However, in this paper, proposed MLI uses Level shifted modulation techniques such as Phase Opposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) techniques. All these techniques works with constant frequency and multiple carrier signals. The switching patterns for all the switches in 15 levels asymmetric MLI is implemented by taking the help of Boolean logical gates as they provides flexibility in operating and increases the probability in implementation of desired switching sequence at specified time intervals.

II. PROPOSED MLI AND MODULATION TECHNIQUES:

In general, MLI are suitable for high voltage and high current applications. These types of inverters offer high efficiency with low THD values. So MLI can be applied to different electric motor drives [6] and utility interface systems to renewable energy sources such as solar, wind with the grid. As the output level increases, the generated output voltage will become almost near to sinusoidal waveform which results in the low harmonic value. In order to produce high voltage levels, large numbers of low voltage devices are used. But In proposed technology with less number of switching devices more levels of output voltage is achieved. Fifteen levels of output voltage are generated with using only seven numbers of power electronic switches as shown in fig.1.

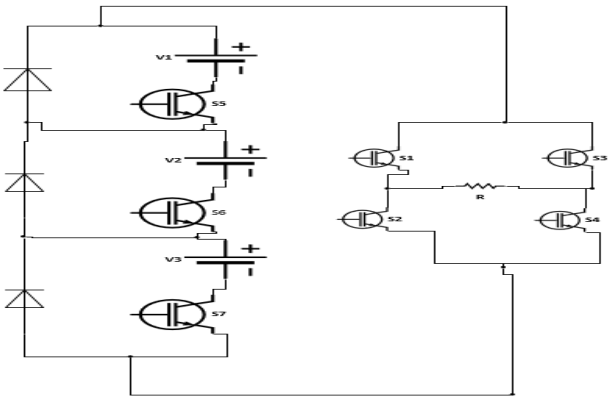

Fig.1. Proposed circuit

Among all the seven switches in the proposed circuit, four switches are used for polarization, which it drives the waveform apart and remaining three switches are responsible for the generation of fifteen levels of output voltage. To get fifteen levels of output voltage, various PWM techniques are available and those are categorized as single carrier sine PWM (SCSPWM), Sub harmonic PWM (SHPWM), Multi carrier PWM and Variable switching frequency PWM are widely used. After careful investigation [7], [8] multicarrier PWM technique is adopted for pulse generation. There are two types in multicarrier PWM, such as phase shifting multicarrier PWM and Level shifting multicarrier PWM.

In this proposed model, level shifting modulation techniques are used such as phase disposition (PD), phase opposition disposition (POD) and Alternate phase opposition disposition (APOD) techniques. To produce fifteen levels of output voltage, it requires (L-1) carrier signals i.e, fourteen carrier signals are required in this particular design.

In Phase disposition (PD), all carrier signals are level shifted and has no phase difference irrespective of the zero reference line as shown in fig.2.

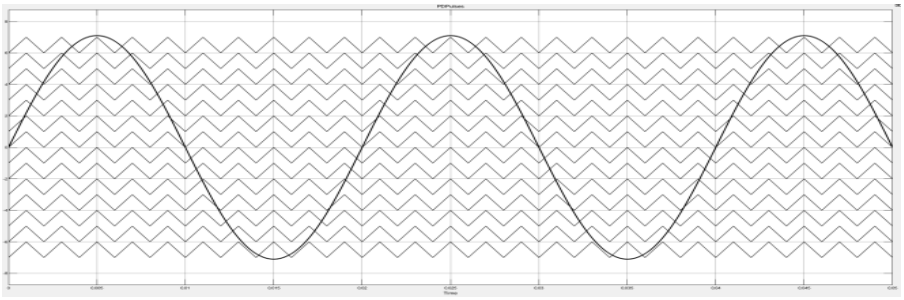

Fig.2. Phase disposition carrier signals

In Phase opposition disposition (POD), all the carrier signals above zero reference line are level shifted and has no phase difference and below zero reference line all the carrier signals are level shifted and has phase difference of 180^0 as shown in fig.3.

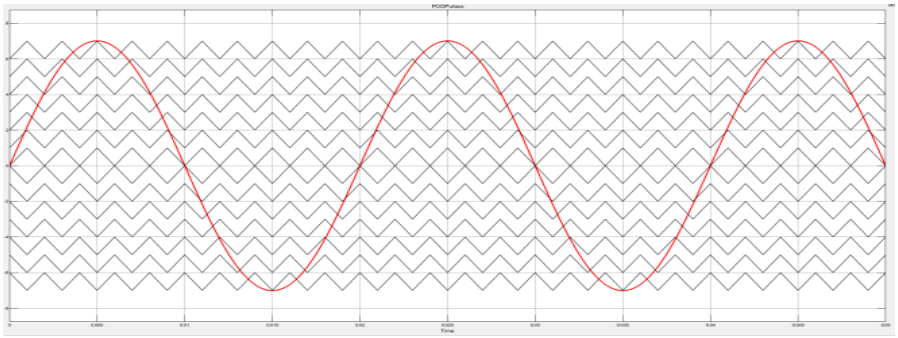

Fig.3. Phase opposition disposition carrier signals

In alternate phase opposition disposition, all the carrier signals are displaced by 180^0 alternatively, irrespective of the reference line as shown in fig.4.

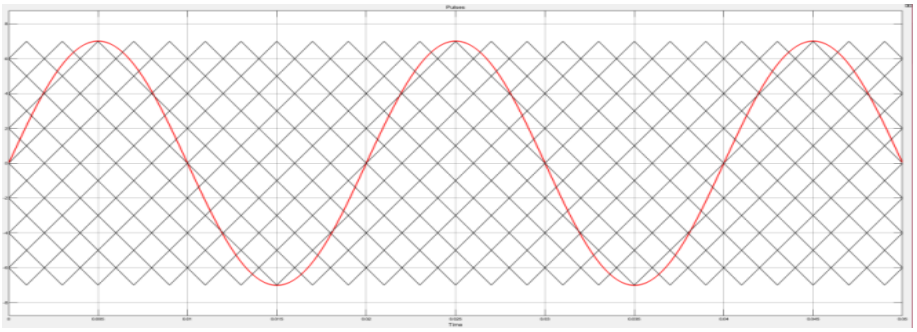

Fig.4. Alternate Phase opposition disposition carrier signals

To generate switching patterns for 15 level MLI's, consider one full cycle of 0.02 seconds, consisting of positive and negative half cycles of 0.01 seconds each shown in fig.5.

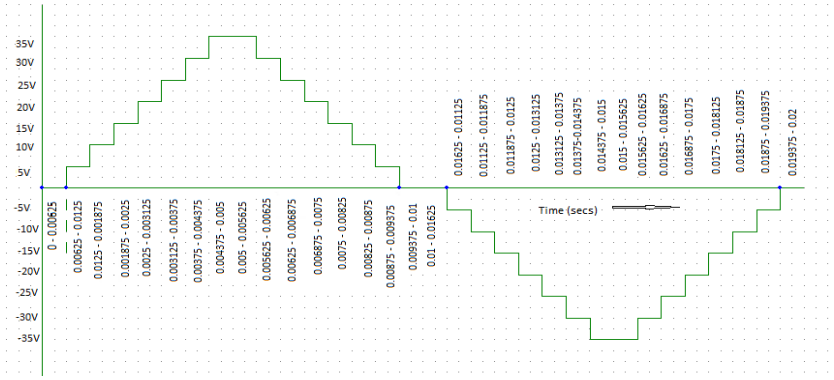

Fig.5. Time divisons of one full cycle for 15 level MLI

III. LOGICAL SWITCHING SEQUENCE:

With the reference to above discussed sections, in order to obtain L level of output voltage, it requires (L-1) carrier signals. Similarly, in the proposed technology 14 carrier signals are required. The designing of switching patterns for different configurations of reduced number in switches are discussed in many papers [9], [10] with the help of modulation techniques. However, it is bit difficult to design such switching patterns for each individual switch at specified time intervals. In such cases, implementation of different Boolean logical gates [11] simplifies the task as it provides flexibility for different states of switching. To generate pulse patterns for fourteen carrier signals, binary representation for asymmetrical Dc voltage sources are considered and tabulated in the table:I along with the switchingsequences.

Table:I- Switching sequence of MLI

Time Divisons (secs)	**Voltages**	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**N1**	**N2**	**N3**	**N4**	**N5**	**N6**	**N7**	**S5**	**S6**	**S7**
0-0.00625	**0V**	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
0.00625-0.0125	**+5V**	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0.0125-0.001875	**+10V**	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0
0.001875-0.0025	**+15V**	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0
0.0025-0.003125	**+20V**	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	1
0.003125-0.00375	**+25V**	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0.00375-0.004375	**+30V**	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0.004375-0.005	**+35V**	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0.005-0.005625	**+35V**	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0.005625-0.00625	**+30V**	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0.00625-0.006875	**+25V**	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0.006875-0.0075	**+20V**	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	1
0.0075-0.00825	**+15V**	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0
0.00825-0.00875	**+10V**	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0
0.00875-0.009375	**+5V**	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0.009375-0.01	**0V**	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
0.01-0.01625	**0V**	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
0.01625-0.01125	**-5V**	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0
0.01125-0.011875	**-10V**	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0
0.011875-0.0125	**-15V**	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
0.0125-0.013125	**-20V**	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1
0.013125-0.01375	**-25V**	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
0.01375-0.014375	**-30V**	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
0.014375-0.015	**-35V**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0.015-0.015625	**-35V**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0.015625-0.01625	**-30V**	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
0.01625-0.016875	**-25V**	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
0.016875-0.0175	**-20V**	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1
0.0175-0.018125	**-15V**	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
0.018125-0.01875	**-10V**	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0
0.01875-0.019375	**-5V**	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0
0.019375-0.02	**0V**	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0

To write switching patterns for S5, S6, S7 using logical gates first divide the switching pattern into positive and negative half cycle. Observe all the positive patterns P1, P2, P3, P4, P5, P6, P7 and required switching pattern, and then choose required logical equation. Similarly repeat the same for negative half cycle and then combine both halves with suitable logical gates in order to obtain required switching patterns. The logical circuit implementation for S5 switch is shown in the fig. 6 and its logical equation is as follows.

S5= (((P1⊕P2⊕P3)⊕P4⊕P5)⊕P6⊕P7) ⊙ (((N1⊕N2⊕N3)⊕N4⊕N5)⊕N6⊕N7)

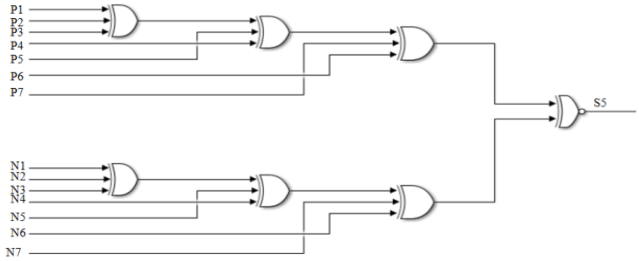

Fig.6. Logical circuit for S5

The logical circuit is shown in fig.7 and logical equation for S6 is as follows

S6= [(P2⊙P4) +P6] + [($\overline{N_2}$ ⊙ $\overline{N_4}$) + $\overline{N_6}$]

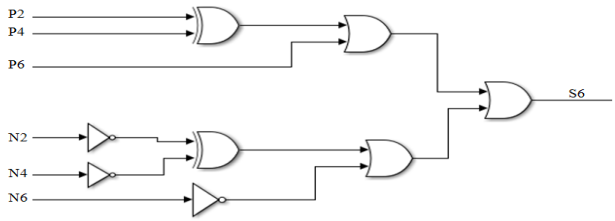

Fig.7. Logical circuit for S6

The logical circuit is shown in fig.8 and logical equation for S7 is as follows

S7=P4+ $\overline{N_4}$

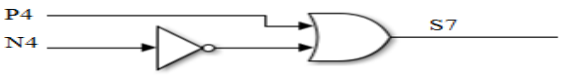

Fig.8.Logical circuit for S7

IV. SIMULATION RESULTS:

The proposed circuit is designed with the aim to generate 15 levels of output voltage which is shown in the fig.9 and the 14 pulse patterns comprising seven positive pulses and seven negative pulses are shown in the fig.10.

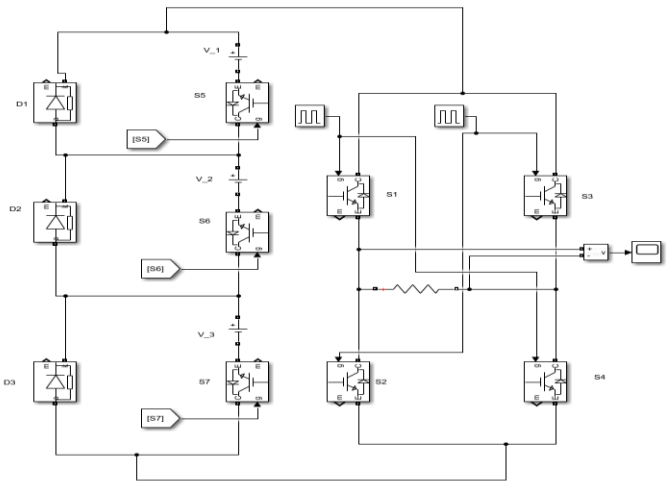

Fig.9. Design of Proposed circuit

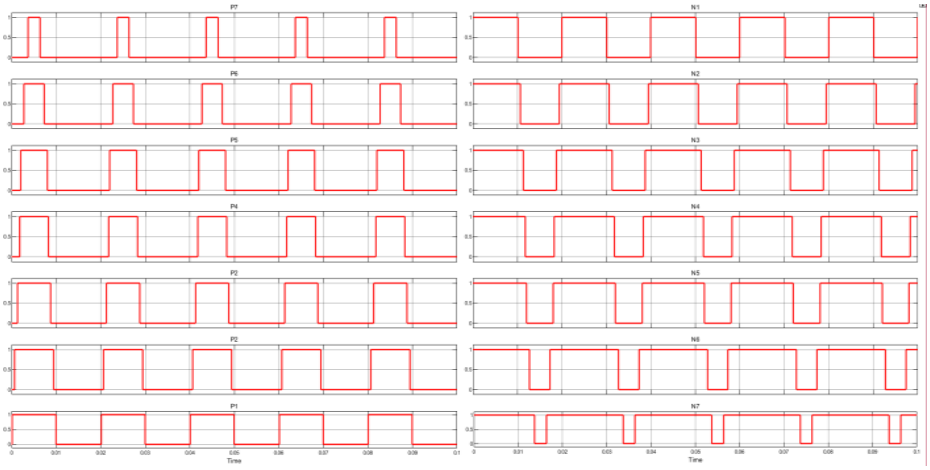

Fig.10. Pulse pattern of 15 levels MLI

The gating circuit is given based on the pulse patterns and Binary code representation, the switching patterns for S5, S6, S7 are written and implemented using logical gates. The resultant output voltage waveform which is having 15 levels of voltage is shown in the fig.11 below.

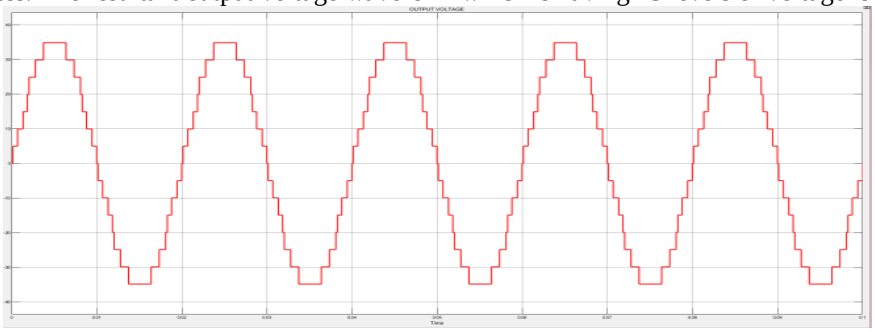

Fig.11 Output voltage waveform of 15 levels MLI

Here, Output voltage waveform is generated by using PD, POD, APOD Pulse Width modulation Techniques. The THD analysis for each of the method is performed and the percentage of harmonic distortions is given in the following fig.12, fig.13, fig.14 respectively.

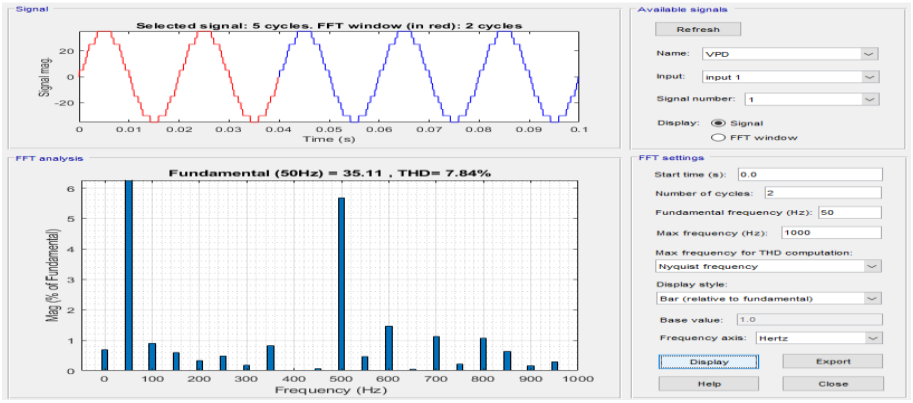

Fig.12.THD analysis using PD technique

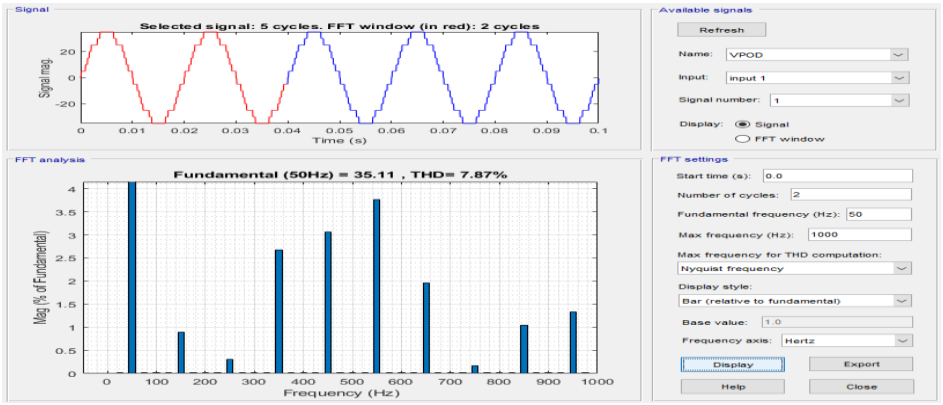

Fig.13.THD analysis using POD technique

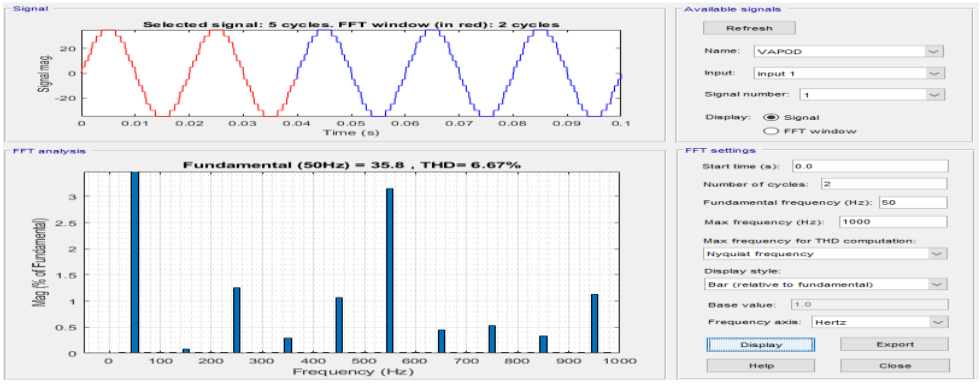

Fig.14.THD analysis of APOD technique

The comparison of PD, POD, APOD modulation strategies for 15 levels MLI is tabulated in table: II as below.

Table-II Comparison of PD, POD, POD techniques

Technique	Fundamental frequency	THD (%)
PD	35.11	7.84
POD	35.11	7.87
APOD	35.8	6.67

V. CONCLUSION

The THD analysis for asymmetrical 15 levels MLI is performed and presented in this paper. It is observed that if the high levels of output voltage are preferred, then the percentage of harmonic distortion decreases with APOD technique as compared to PD and POD modulation techniques. For low level inverters, PD technique [12] is suitable as it gives less THD than POD and APOD techniques. The less harmonic distortions in the circuit results in high efficiency with more quality which is suitable for many applications.

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