One-Sided Schmitt-Trigger-Based 9T SRAM Cell for Near-Threshold Operation

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i)Abstract:

SRAM is the most popular memory elements it is used in mainly digital devices. SRAM consists of various types like 6T,7T,8T,9T. And it consists of static noise margin(SNM) and write margin(MW),Delay and power consumption. Here 6T SRAM cell consists of 6 transistors because the name indicates 6T.6T is used to store the information in 6T we use two bit lines because to perform better noise margin. In single bit there is less noise margin so we considered two bit lines.7T SRAM cell consists of 7 transistors there is disadvantage in 6T so we use 7T. The disadvantage is that read line charges slowly. In 7T read line charges very fast and power consumption is less. power consumption of 7T is 42mw and delay is 4.9ns.8T consists of 8 transistors 8T is same as 6T difference is that only one internal inverter.8T SRAM cell power consumption is 67mw and delay is 6.8ns.9T consists of 9 transistors. power consumption is 71mw and delay is 8.05ns. Compared to 6T,7T,8T the 9T SRAM Cell has more power consumption so we use 9T SRAM cell.

KEYWORDS: Bit interleaving, low energy, near-threshold, Schmitt-trigger, static random access memory (SRAM).

1. Introduction:

SRAM is defined as static random access memory. SRAM is constructed by using CMOS technology. It consists of 4 to 6 transistors. Transistors uses clocks. Because clocks holds the data. In SRAM gate and subthreshold leakage of currents are present so, that it decreases the static power. Whenever we increases the ground level then it decreases the subthreshold leakage during inactive mode. SRAM is a volatile memory it looses data when the power goes down. Whatever input we are giving to a computer will be converted in the form of 0's and 1's similarly output generated by the computer is binary language. SRAM has that the memory part in hardware low power modeling plays an important role in energy consumption. SRAM memory has several methods to save power such as pipelining, redundancy, data encoding, and clocking. SRAM has 6 transistors where as 2 transistors among 6 transistors are pass transistors. Which provides excess to the bit lines and other 4 transistors are two cross coupled inverters among which T1, T2 is CMOS inverter pair and another T3, T4 are CMOS inverter pair. SRAM presents the idea of modifying cryptography hardware.

2. Literature survey:

This is to analyse the static noise margin (SNM) of 6T SRAM cell during read operation is increase in transistor using 180nm technology. We can overcome the power consumption due to additional transistor. We use 6T SRAM in 45nm CMOS technology to provide interface with CPU. We can overcome the large fraction of total power in SRAM cell. Here, we can provide lo leakage power using self controlled voltage level circuits in 9T SRAM these results in average power. In the design of 9T SRAM cell can consume less power and high read stability. When we compared to other technology there is a decrease in power and increases in stability. Here we can reduce 87% of

power during write operation, 66% of power during hold operation and 85% of power in read operation. The power is reduced only proportionally to the supply voltage.

3.DESIGN AND SIMULATED PROPOSED TECHNOLOGY:

i)WRITE OPERATION:

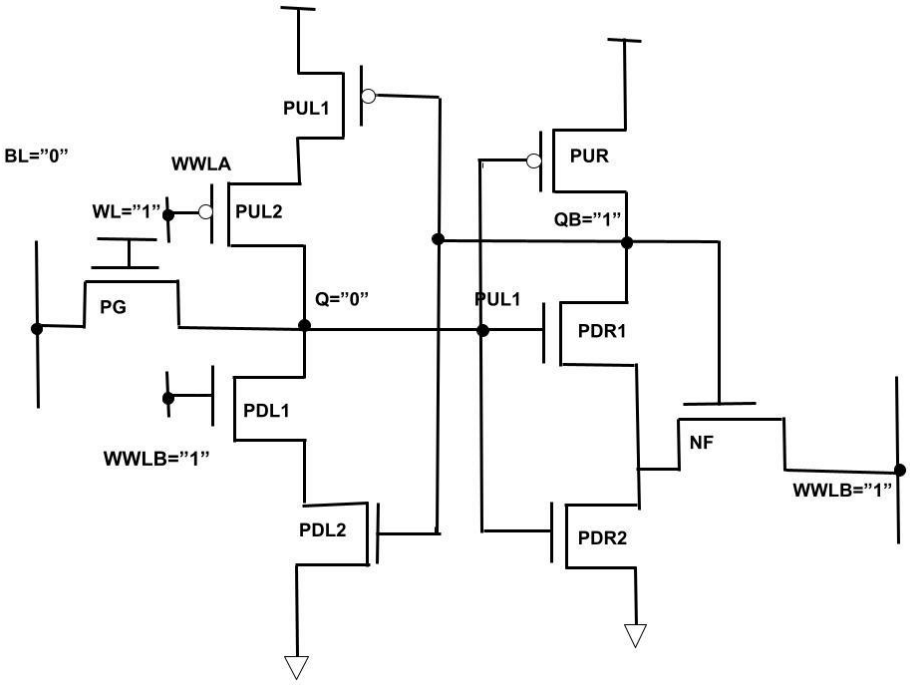

Fig A: Write operation

In previous Technology they used 22nm Technology But in this project we are using 16nm Technology because by using less technology we gain more power consumption and stability so we used 16nm in this project. Here BL=0 and WL=1.Q=0 directly connected to PDR1 then it should be OFF condition.PDR2 is connected to ground remains 0.WWLB remains "1", the write driver drives BL to "0", and the WL is enabled. WWLA is changed to "1" it is not connected to the path from the VDD power source by turning off PUL2, node Q storing data "1" is power gated. WWLA is reset to "0" after the stored data of node QB is flipped.

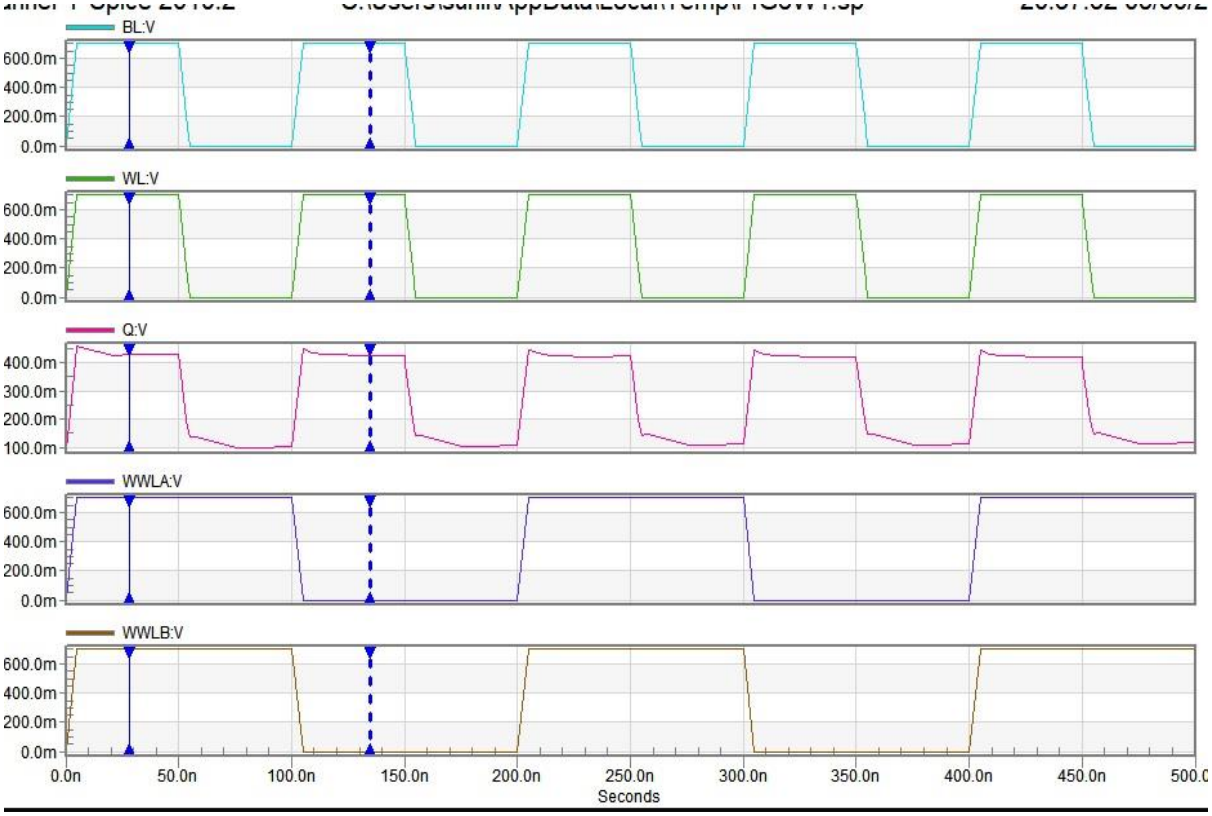

Fig B: Wave form for write operation

To simulate or work the 9T SRAM values are given as, DC voltage of 9T SRAM cell is 1.8v, the inputs of voltage 1 and voltage 2 are V1 = 0v and V2 = 1.2v. The period of 9T SRAM cell is 200 n/s. Delay time of 9T SRAM is 100ns Rise time of 6T SRAM is 100 p/s. Fall time of 9T SRAM is 100 p/s. And the pulse width is 25 n/s.

VV1 from time 0 to 5e-07

Average power consumed is 9.712658e-08 watts

Max power consumed is 6.375612e-06

Min power consumed is 1.774740e-08

Power delay product= Avg Power*Delay

ii)READ OPERATION:

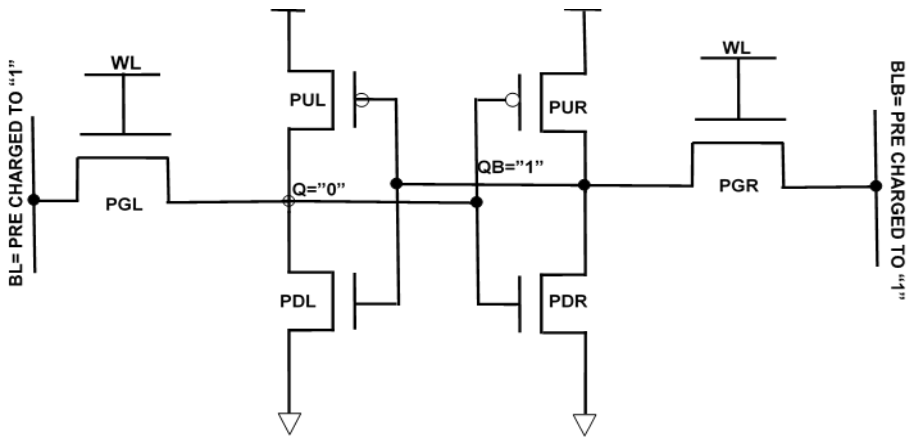

Fig C: Read operation

Here we have 6 Transistors. And by connecting two transistors we formed an inverter. we have BL and BL bar. BL is an input, BL bar is an output. BL and WL is connected to transistor 1.where as WL is Word Line. where BL bar and WL is connected to transistor 6.And both the drains are connected to ground and both sources are connected to VDD. And we have to print the output by using output supply. Here BL is 0 transistor T5 is On and T6 is Off condition. Then output becomes 1(VDD) then VDD is connected to inverter which forms by using transistor T1 and T2.Then T1 is Off and T1 is ON, as we know that T1 is connected to ground then the output becomes 0 Automatically.

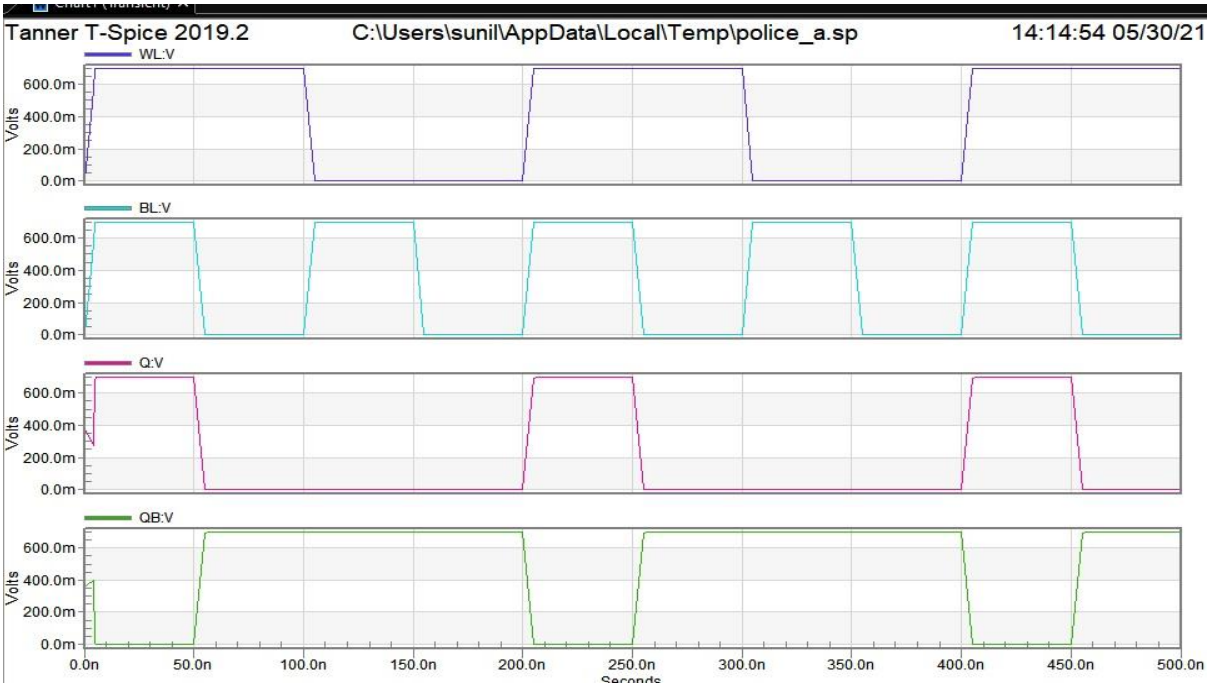

Fig D: Wave form for read operation

To simulate or work the 6T SRAM values are given as, DC voltage of 6T SRAM cell is 1.8v, the inputs of voltage 1 and voltage 2 are V1 = 0v and V2 = 1.2v. The period of 6T SRAM cell is 200 n/s. Delay time of 6T SRAM is 100ns Rise time of 6T SRAM is 100 p/s. Fall time of 6T SRAM is 100 p/s. And the pulse width is 25 n/s.

VV1 from time 0 to 5e-07

Average power consumed is 9.712658e-08 watts

Max power consumed is 6.375612e-06

Min power consumed is 1.774740e-08

Power delay product =Avg Power*Delay

4.RESULT:

Finally we conclude that 9T SRAM cell is Best compared to the 6T 7T 8T.And by using different references we got more knowledge about this project.

SRAM cell	22nm	16nm
Vin	0.48 V	0.7 V
Delay	8.2 ns	6.3 ns
Power consumption	7.61248 watts	9.712658e-08 watts
PDP = Avg power * delay	62.32J	61.17J

5.CONCLUSION:

Low energy consumption has become important for bio implants and mobile devices because they need to operate with limited energy. For minimization of the energy consumption, it is important to operate the SRAM in near-Vth region. This paper proposed a one-sided ST 9T SRAM cell with low energy consumption, and high read stability, write ability, and hold stability yields in the near-Vth region. The read stability yield was improved in the proposed ST 9T SRAM cell by using a cross-coupled structure of standard and ST inverters. In addition, the proposed ST 9T SRAM cell ensured a 5σ target write ability yield by using selective power gating and a novel negative VWWLB assist technique that controlled the trip voltage of the ST inverter.

6.REFERENCES:

[1] B. Calhoun and A. Chandrakasan, "Static noise margin variation for sub-threshold SRAM in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1673–1679, Jul. 2006.
[2] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming Moore's law through energy effificient integrated circuits," *Proc. IEEE*, vol. 98, no. 2, pp. 253–266, Feb. 2010.
[3] B. H. Calhoun, J. F. Ryan, S. Khanna, M. Putic, and J. Lach, "Flexible circuits and architectures for ultralow power," *Proc. IEEE*, vol.98, no. 2, pp. 267–282, Feb. 2010.
[4] R. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 305–316, Sep. 2005.
[5] M.-H. Chang, Y.-T. Chiu, and W. Hwang, "Design and iso-area V*min* analysis of 9T subthreshold SRAM with bit-interleaving scheme in 65-nm CMOS," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 59, no. 7, pp. 429–433, Jul. 2012.
[6] P. Hazucha *et al.*, "Neutron soft error rate measurements in a 90-nm CMOS process and scaling trends in SRAM from 0.25-mm to 90-nm generation," in *IEDM Tech. Dig.*, Dec. 2003, pp. 21.5.1–21.5.4.
[7] I. J. Chang, J.-J. Kim, S. P. Park, and K. Roy, "A 32 kb 10T subthreshold SRAM cell array with bit-interleaving and differential read scheme in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 650–658, Feb. 2009.
[8] L. Chang *et al.*, "An 8T-SRAM for variability tolerance and low-voltage operation in high-performance caches," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 956–963, Apr. 2008.
[9] G. Pasandi and S. M. Fakhraie, "A 256-kb 9T near-threshold SRAM with 1k cells per bitline and enhanced write and read operations," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 11, pp. 2438–2446, Nov. 2015.
[10] J. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based sub-threshold SRAM cell," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.
[11] M.-H. Tu *et al.*, "A single-ended disturb-free 9t subthreshold SRAM with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1469–1482, Jun. 2012.
[14] T. W. Oh, H. Jeong, K. Kang, J. Park, Y. Yang, and S.-O. Jung, "Power-gated 9T SRAM cell for low-energy operation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 3, pp. 1183–1187, Mar. 2017.
[15]C. Auth *et al.*, "A 22 nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *Proc. Symp. VLSI Technol.*, Jun. 2012, pp. 131–132.
[16]C.-H. Jan *et al.*, "A 22 nm SoC platform technology featuring 3-D tri-gate and high-*k*/metal gate optimized for ultra low power high performance and high density SoC applications," in *IEDM Tech. Dig.*, Dec. 2012, pp. 3.1.1–3.1.4.