IJRAR.ORG E-ISSN: 2348-1269, P-ISSN: 2349-5138

INTERNATIONAL JOURNAL OF RESEARCH AND ANALYTICAL REVIEWS (IJRAR) | IJRAR.ORG

An International Open Access, Peer-reviewed, Refereed Journal

Matlab based Loeffler Algorithm Implementation for Image Coding by accelerating DCT/IDCT performance

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ABSTRACT

Previously there is use of DCT (Discrete Cosine Transform) and IDCT (Inverse Discrete Cosine Transform) are used for image analysis. It is observed that DCT/IDCT are not much efficient for image analysis. So in this application we have introduced blocks based (8x8) DCT and IDCT along with advanced Loeffler Algorithm which provides better efficiency for image analysis. This proposed architecture even gives performance very fast and error prone. This same application can be analyzed in future with hardware like FPGA for real time analysis. In this application we considered multiple images for analysis. The performance is observed by both subjective and objective ways. Subjective way includes the human visualization while objective way includes different parameters such as PSNR, MSE, time consumption, etc.

Index terms: FPGA, Loeffler's Algorithm, Image coding, PSNR, MSE and time consumption.

I. Introduction

The rapid rise of computer IT has resulted in a considerable demand for portable multimedia devices in recent years [1]. These devices are subject to strict specifications regarding memory, power consumption, and available resources. High-quality, high-resolution digital pictures and video data require real-time processing [2].

Due to their superior energy compression performance, inverse discrete cosine transforms (IDCT) and discrete cosine transforms (DCT) are used in a number of image and video coding applications, such as H.26x [7], and [8] MPEG [4]–[6], and JPEG [3], Even though there have been quicker techniques in the past to compute 8-point 1D DCT/IDCT, most of them required performing 12–13 multiplications and 29 additions [10]–[15].

When performing 2D DCT/IDCT computations, transforming two 1-D sequences— columns and rows —is a common breakdown. A transpose matrix is required in order to capture the 1D DCT/IDCT transformation coefficients. For the hardware implementation of 2D DCT/IDCT, there are 2 main categories of approximation designs: fixed-point operations [24]–[28] and algebraic integer coding [20]–[23]. Algebraic integer encoding is used to transform the real cosine values into a set of integers. The encoding of these integers into an immovable point approximation form (FRS) is then handled by the final reconstruction stage.

1.2 LOEFFLER TRANSFORM ALGORITHM

For a N×N pixel matrix, the computation of the 2D DCT/IDCT [29] is defined as

$$y(u,v) = \frac{2c(u)c(v)}{N} \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} x(i,j) \cos\frac{(2i+1)u\pi}{2N} \, Cos\frac{(2j+1)v\pi}{2N} \qquad (1)$$

II. LITERATURE SURVEY

M. Masala, E., Siekkinen, J. Improved upload techniques for real-time, scalable video streaming from mobile devices

Among smartphone users, sharing live multimedia material is becoming an increasingly popular practice. In this study, we examine the issue of chunked video content and the use of scalable video coding (SVC) to optimise video quality in such cases. We contemplate limiting our application to common stateless HTTP servers that don't need additional video content processing. Our main contribution is to offer nearly ideal algorithms for scheduling video segment uploads for several clients with various viewing latency times.

Dealing with such a group of clients creates challenges in determining which chunks to upload first and in what sequence to achieve the greatest possible balance between quality and latency. Through simulations, we demonstrate that under real-world scenarios, the suggested algorithms can achieve much better performance than naive techniques. [1]

A. Shabani, B. Khabbazan, S. Sabri, and M. Sabri. Timarchi, "Variable-sized DCT architecture for HEVC with area and power efficiency using muxed-MCM problem,"

For HEVC applications, this study offers a space- and power-efficient variable-size DCT design. We leverage the Muxed-MCM issue to design a scalable and reconfigurable shift-and-add unit (SAU) that is integrated into our 1D-DCT architecture, thereby lowering hardware cost and increasing hardware reusability in the arithmetic units. The fundamental concept of the suggested design is that lower point DCTs are executed approximately 90% of the time and higher point SAUs are not employed.

Even with its more intricate design, HEVC offers superior coding efficiency since its primary transform employs DCT computation for many transform sizes, ranging from 4 × 4 to 32 × 32. This study offered a practical way to lower the hardware complexity in a space-saving, variable-sized DCT design for high-efficiency video coding. Through the use of the Muxed-MCM job, we offered a scalable Solution. [2]

G. K. Wallace, "The standard for JPEG still picture compression," IEEE Trans. Eat. Electron., no. 38, no. 1, Feb. 1992, pp. 18–34.

For continuous-tone still photos, including colour and grayscale, the joint ISO/CCITT body JPEG (Joint Photographic Experts Group) is in responsibility of creating the first global compression standard. The proposed JPEG standard seeks to serve a wide range of continuous-tone image applications and eventually become ubiquitous.

The JPEG standard includes two fundamental compression techniques, each with different modes of operation, to accommodate the diverse requirements of a broad range of applications.

For "lossy" compression, discrete cosines transform (DCT)-based approach is provided; for "lossless" compression, a predictive strategy is advised. To date, the most used JPEG approach is the Baseline technique, which is enough for many purposes on its own. The Baseline is the main topic of the author's overview of the JPEG standard. [3]

K. Brandenburg and G. Stoll, "A generic standard for coding high-quality digital audio: ISO/MPEG-1 audio," J. Sound Engineer.

The standard paradigm for these systems is based on filter banks and is quantized and coded using a human hearing model as guidance. The paper presents the underlying technology, the theoretical foundation for optimality verification, and the most widely recognised standards, which are grounded in more recent studies and basic ideas.

One of the most prominent examples of disruptive technology is generally accepted to be audio coding that is both high-quality and low-bit-rate. Some even claim that the demise of the music industry as we know it was caused by audio coding. In recent years, audio coding has proven to be a very successful digital signal processing method for both technology and business. [4]

III. PROPOSED METHOD

A. REDISTRIBUTION OF LOEFFLER DATA STREAMS

Even though the Loeffler computation has determined the theoretical minimum for the diverse range of additions and subtractions, the estimate measure for every clock cycle is inconsistently provided. The structure (five C 6) · b C (g − b) · 6 retains two duplicates and several additions for the primary heading, hence affecting the circuit design machine's operating speed.

The growth and augmentation inside the rule arrangement should be carried out in a sequential manner, considering the connection between the records distribution. Consider the fact that sequential clock input pixels are used by the 2D DCT/IDCT transformation circuit in real-world image and video pressure handling applications.

For a 1D DCT/IDCT module, it takes eight clock cycles to secure a line of pixels in an eight-by-eight length picture block. Every four clock cycles, the first Loeffler calculation completes the change of a line of pixels. At that time, within 8 cycles, it wishes to stand for 4 cycles before starting the change of the next column of pixels.

B. MULTIPLICATION-FREE OPERATION Number augmentation by fixed-factor guess assessment replaces the drifting variable activities entirely within rule arrangement are fixed constants. The transmission of marked lessens the range of actions involved in the shift augmentation. One might shift them into the condition of subtracting one from the force of two by connecting more than three "1" twofold attributes.

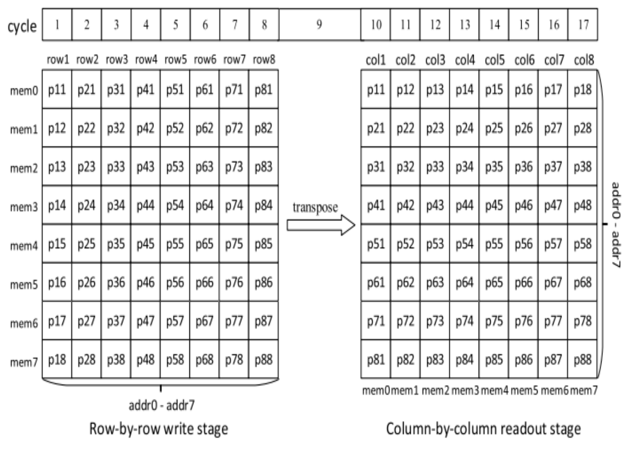

Figure 3: Transposing an 8 × 8 matrix row-column parallel.

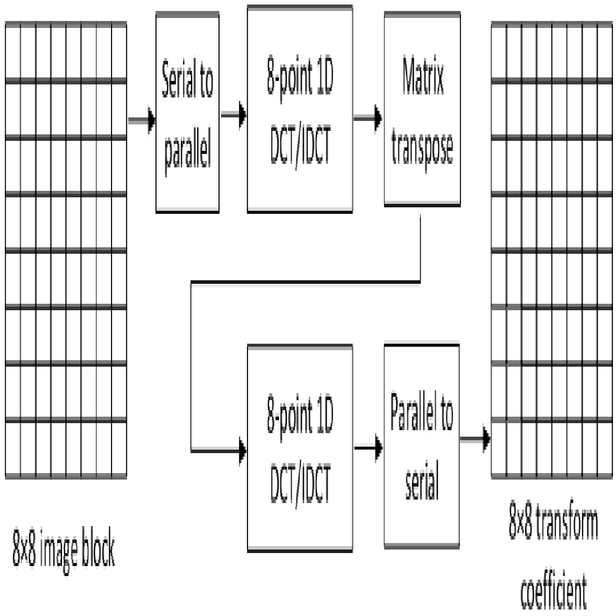

Figure 4: Diagram of the 2D DCT/IDCT structure.

C. PARALLEL TRANSPOSE MATRIX

In order to bring the section to a 64-force Slam, Fig. 2 illustrates how the correct technique uses a sequential clock to synchronise an unmarried pixel on an eight-by-eight picture block. The addresses numbered 1 through 8 correspond to the grid's basic line, whereas those numbered 9 through 16 correspond to the framework's second column.

D. HARDWARE IMPLEMENTATION OF 2D DCT/IDCT

The condition of the 2D DCT/IDCT is proposed in Fig. 4, which includes the sequential to resemble (SP), network translate (MT), lined up with sequential (PS). Initially, the 8 × 8 image block uses the SP unit to execute realities grafting on a column of 8-factor pixels. This causes the line pixels to cycle through and eventually end up in the first-stage eight-factor 1D DCT/IDCT unit for line change.

After completing the line section rendering, the MT unit sends the segment, which is a one-degree eight-factor unit, for segment modification. Finally, the PS unit yields the equal realities into positions such as the revamp coefficient framework, cycle by cycle. The SP and PS devices confirm that there are no issues with the sequential and equal transformation between eight-by-eight image block records streams.

HARDWARE ARCHITECTURE:

The eight-point DCT's equipment design with a better Loeffler set of regulations is seen in Fig. 5. The whole design eight-level sign a comparable expansion, deduction, duplication task to its greatest advantage. During step 1, the entry realities x0 − x7 are communicated, subtracted individually, and then stored inside the resultant degree sign-in. One important method for requiring large course calculation parting is the growth of registers 8 and 9.

Table 6's CSD coding implications use the comparative normal components degree. Since the consistent item is repeated outcome adjusted at some point in degree 8 to lessen the comparison discrepancy. Figure 6 illustrates the eight-point IDCT's equipment engineering.

The coefficients following DCT are represented by the entry records y0 through y7, and the coefficient registers must be switched places before the activity is completed. The equipment design data development may be reorganised when the DCT converse activity (refer to Fig. 5) moves from degree 8 to degree 1.

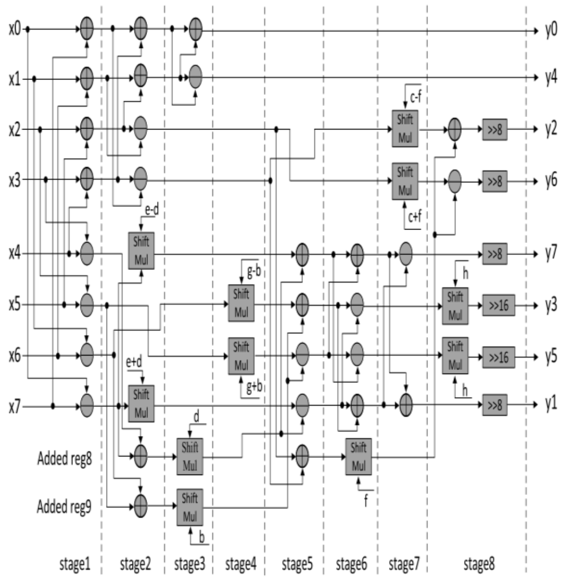

FIGURE 5. 8The hardware structure schematic of the 8-stage DCT pipeline is shown.

IV. RESULT

Here we used matlab software for proposed model design. This model even further can be implemented using hardwares likes FPGA to understand real time working. Matlab software is choosen for this application as its user-friendly and many relevant tools are available for image and video processing.

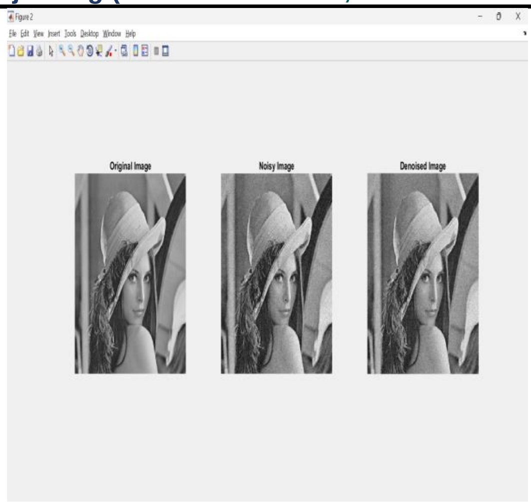

Fig.5.1 Existing Implementation a) Original Image b) Noisy Image c) Applied DCT/IDCT

In this we selected original image as lena image and then replicative noise is added and then applied DCT/IDCT to understand the performance.

It is observed that performance of existing techniques is poor as image is not analysed with efficient way.

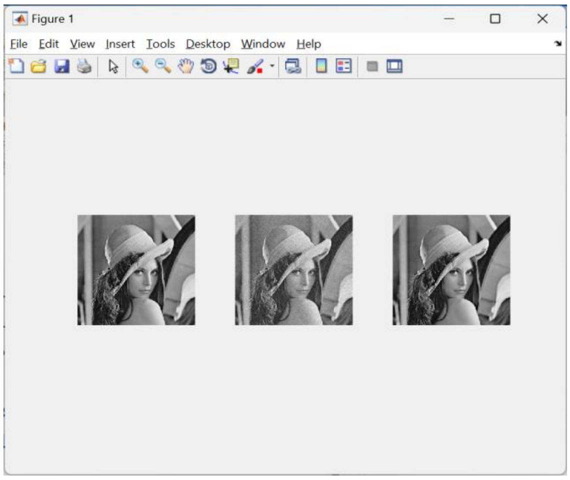

Fig.5.2 Proposed Implementation a) original image b) Noisy image c) proposed Loeffler DCT/IDCT

In this we selected original image as lena image and then replicative noise is added and then applied extension Loeffler based DCT/IDCT to understand the performance.

It is observed that performance of proposed techniques outperforms as image is analysed with efficient way and the time required is very less.

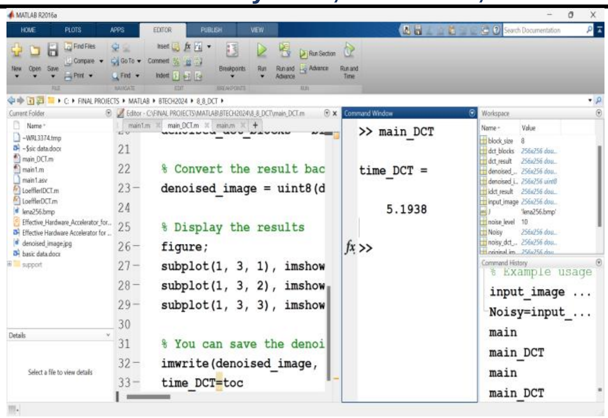

Fig.5.3 Time for DCT/IDCT Processing

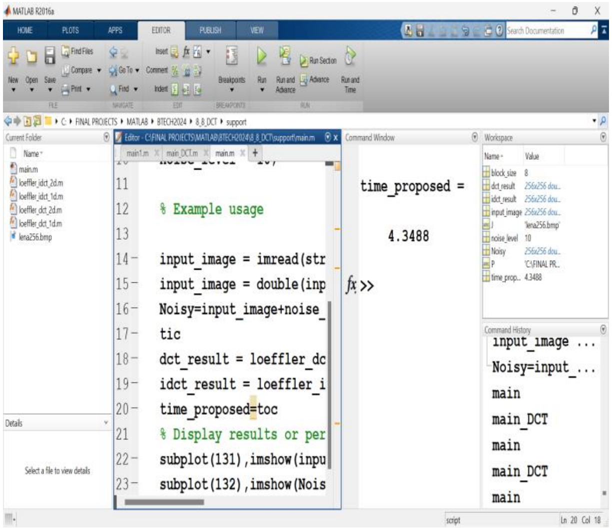

Fig.5.4 time required for Proposed model for processing

By both subjective and objective way, it is observed that proposed model is performing superior that state of art technique.

V. Conclusion

In this project we have implemented efficient as well as fast architecture for image coding. The proposed architecture outperforms the existing DCT/IDCT. In proposed method 8X8 block-based architecture is implemented for DCT/IDCT with enhancement using Loeffler algorithm. This parallel architecture is applied to image for faster processing and better efficiency. This proposed application is suitable for both image coding as well as video coding. The performance of proposed algorithm is displayed using PSNR, MSE and processing time. All the above three parameters outperform the existing techniques.

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